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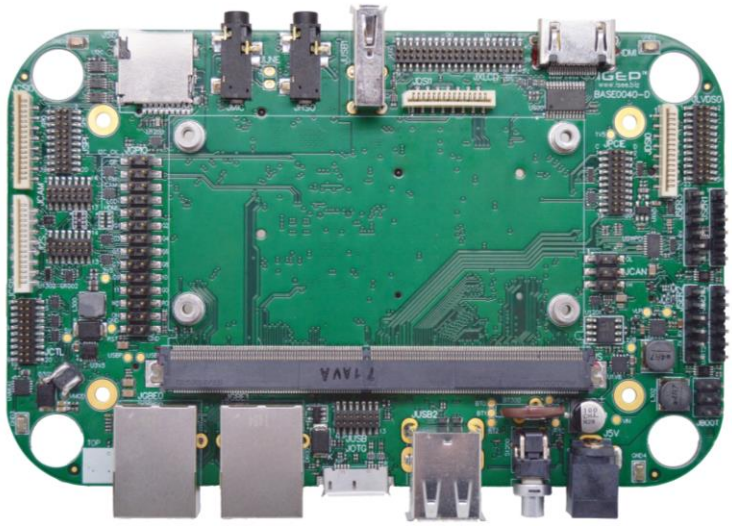

IGEP™ SMARC EXPANSION

HARDWARE REFERENCE MANUAL

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

IATEC

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1.0	05/26/2017	• Preliminary Revision (BASE0040-RAxx)
1.1	05/29/2018	• Design Changes
2.0	11/12/2019	• Second Release (BASE0040-RDxx)

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1 USER INFORMATION

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2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The BASE SMARC EXPANSION is a fully tested, highly reliable, efficient and high performing base board made for development purpose that allows to the Users a total access to the IGEP™ SMARC processor boards family functionalities. With this expansion board, the Users can develop and test their final applications before building a dedicated prototype, saving costs and time-to-market.

This expansion board is designed for Industrial and Commercial purposes and can be used with the complete portfolio of products, so the Users can use the BASE SMARC EXPANSION to test all the processor boards of IGEP™ SMARC family and make easy scalability if it is needed a processor with different specifications.

Highlights:

- 2x Gigabit Ethernet (10/100/1000 Mbps) connectors.
- 1x USB 3.0 HOST/OTG port.
- 3x USB 2.0 Host ports.
- 1x USB expansion port.
- 1x USB modem interface.
- 1x HDMI output.
- 1x LVDS expansion output.
- 2x DSI output.
- 1x LCD output with Touchscreen.
- 1x Line In/Mic audio mini jack.
- 1x Line Out audio mini jack.
- 2x Serial audio ports (I2S).
- 2x Serial camera input (MIPI-CSI).
- 2x CAN bus ports.
- 1x mSATA.
- 1x SIM-Card connector.
- 1x Micro-SD card connector.
- 4x Serial header expansion.
- 2x PCIe ports.
- 1x SPI interfaces.
- 1x Button with two integrated LEDs (Red/Blue).
- 1x Boot select header.
- 5x I2C bus.
- 12x GPIO pins.
- Compatible with SMARC modules.

Note: The BASE EXPANSION BOARD only expands features of the module. All previous features only will be available if are present on the module.

2.2 IGEP™ SMARC BASE EXPANSION BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ SMARC BASE EXPANSION series. Reducing the implementation time and saving costs on their designs. Amongst others, the main benefits are the following:

- Easy scalability between different modules (even with other processors) thanks to the SMARC standard.
- Compact and powerful core for new products.
- Robust and easy to mount due to the MXM3 314-pin connector.
- Reduced time to market.
- Low power consumption: Typical 1W
- Industrial Temperature Range -40 to +85ºC.
- Extended life range product.

At the same time, it can be implemented in all kind of end applications. The followings are just a few ones, but the list can be as long as the imagination of the developers.

- Connected vending machines.
- Home / Building automation (IoT applications).
- Human Interface.
- Industrial Control.
- Test and Measurement.
- Artificial Intelligence

2.3 SMARC STANDARD

The IGEP™ SMARC BASE EXPANSION accomplish the SMARC 2.0 version, which is defined by SGET.

The SMARC (“Smart Mobility Architecture”) is a computer Module definition targeting applications that require low power, low costs, and high performance. This standard is based on the former ULP-COM standard (Ultra Low Power Computer-on-Modules). The Modules will typically use ARM SoCs (System on Chip) families or similar.

SMARC standard defines two module sizes (82mm x 50mm and 82mm x 80mm). **All the available IGEP modules sizes 82mm x 50mm**. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin (156 on TOP side and 158 on BOTTOM side) right angle connector. The module pins are designated as P1-P156 on the TOP side and S1 – S158 on the BOTTOM side. The connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key (4 on the TOP side and 3 on the BOTTOM side).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

2.4 SMARC FORM FACTOR FEATURE SUMMARY

Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards.
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out.
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom).
    - Other stack height options available, including 2.7mm, 5mm, 8mm.
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm.
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector.
- Module input voltage range: 3.0V to 5.25V
  - Allows operation from 3.6V nominal Lithium-ion battery packs.
  - Allows operation from 3.3V fixed DC supply.
  - Allows operation from 5.0V fixed DC supply.
  - Single supply (no separate standby voltage).
  - Module power pins allow 5A max.
- Low power designs
  - Fanless
  - Passive cooling
  - Low standby power
  - Design for battery operation
  - 1.8V default I/O voltage

2.5 IGEP™ SMARC BASE EXPANSION SERIES

The BASE SMARC BASE EXPANSION is a fully equipped baseboard that access to almost all IGEP™ SMARC modules functionalities. It has been designed to be used as the fastest way to develop and check the user's final application before building a prototype, saving costs and reducing time to market.

This model can be used with all the IGEP™ SMARC series modules. Thanks to this design, the user only needs to purchase one Expansion board to check all SMARC modules manufactured by IATEC.

2.6 PARTS NUMBERS

The module configuration defines the part number.

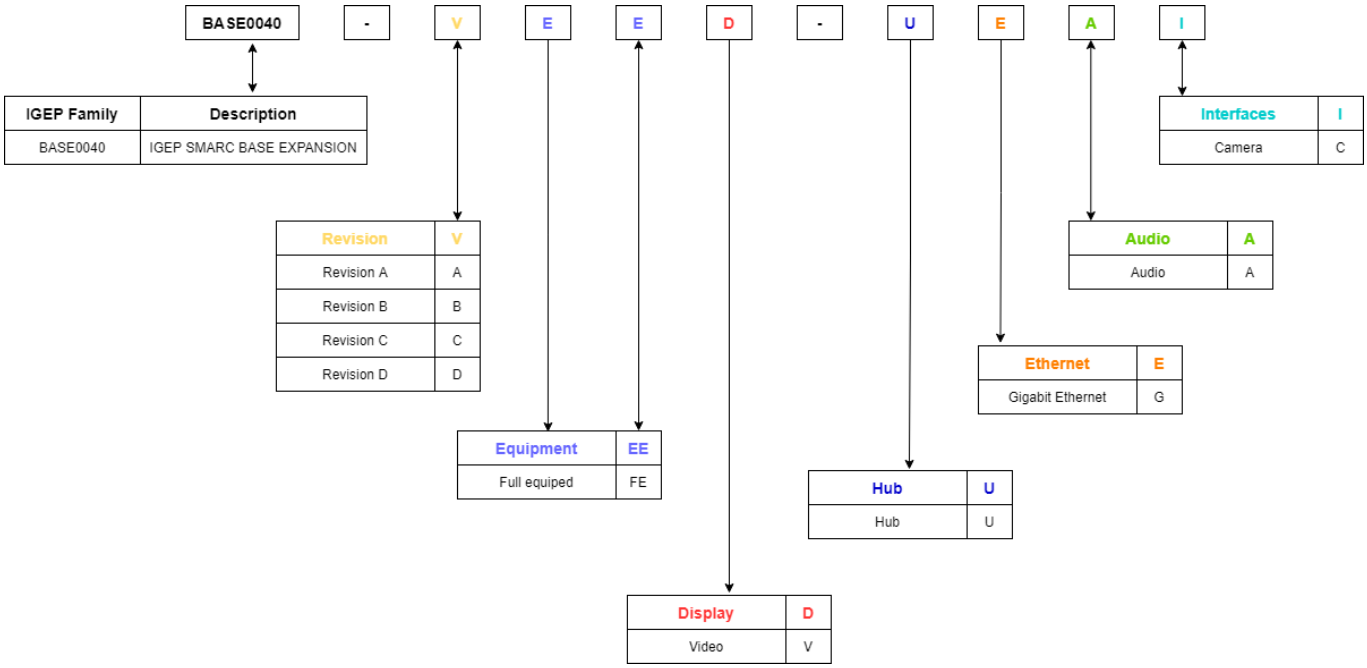


Figure 1 IGEP™ SMARC BASE EXPANSION Part Number

Part Number	IGEP™ Device	Description
BASE0040-DFEV-UGAC	BASE SMARC EXPANSION	Designed for fast prototyping of user's projects.

Table 1 IGEP™ SMARC BASE EXPANSION Ordering Information.

3 HARWARE OVERVIEW

3.1 IGEP™ SMARC BASE EXPANSION

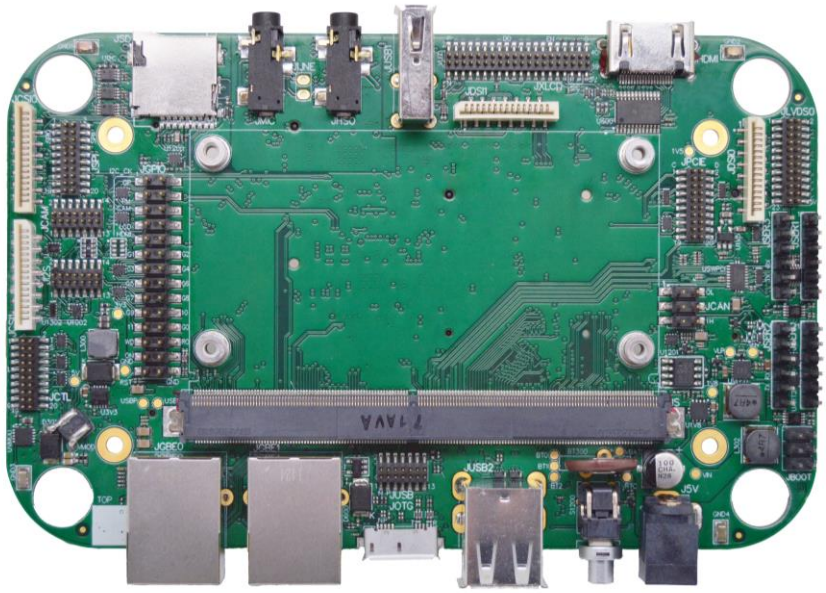


Figure 2 SMARC BASE EXPANSION – Top View

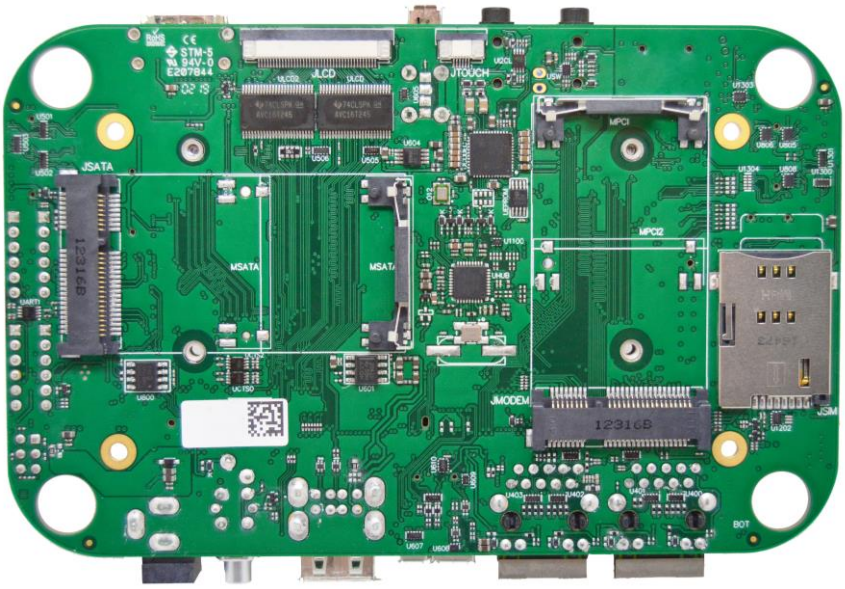


Figure 3 SMARC BASE EXPANSION – Bottom View

3.2 IGEP™ SMARC BASE EXPANSION BLOCK DIAGRAM

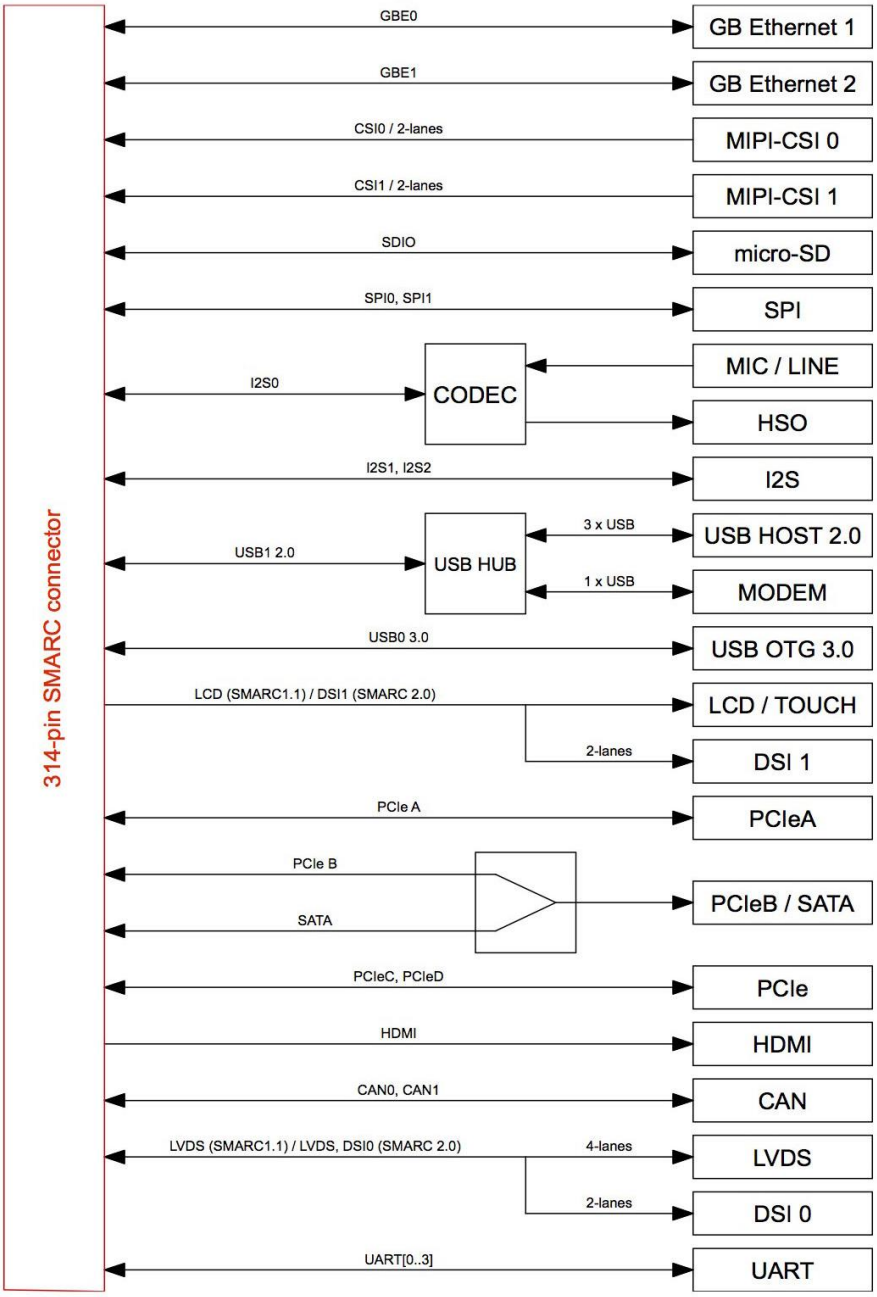


Figure 4 IGEP™ SMARC BASE EXPANSION Block Diagram

3.3 IGEP™ SMARC BASE EXPANSION FEATURES

Feature	Specifications	Conector
Display	1x HDMI Output type A receptacle	JHDMI
	2x DSI connector 15-pin FPC connector (1,00 mm pitch spacing)	JDSI0, JDSI1
	1x LVDS expansion 24-pin header (2x12-pin, 1,27 mm pitch spacing)	JLVDS0
	1x RK050BR62-CT, by Rocktech Displays Ltd (2)	
	1x LCD 24-bit 40-pin FPC connector (0,5 mm pitch spacing)	JLCD
	1x Touchscreen 6-pin FPC connector (0,5 mm pitch spacing)	JTOUCH
	1x User's LCD+Touchscreen (3)	
	1x LCD expansion 40-pin header (2x20-pin, 1,27 mm pitch spacing)	JXLCD
Camera Interface	2x CSI connector, 2-lanes 16-pin FPC connector (1,00 pitch spacing)	JCSI0, JCSI1
	1x Parallel Camera expansion 14-pin header (2x7-pin, 1,27 mm pitch spacing)	JCAM
Digital Audio	1x Stereo Line Input Mic/Line 3,5 mm Jack connector	JMIC
	1x Stereo Line Output Headphone 3,5 mm Jack connector	JHSO
	1x I2S 14-pin header (2x7-pin, 1,27 mm pitch spacing)	JI2S
Network	2x 10/100/1000 Mbps base T RJ45 connector	JGBE0, JGBE1
USB	1 x USB 3.0 Host/OTG, type micro AB receptacle	JOTG
	3 x USB 2.0 Host, type A receptacle	JUSB1, JUSB2
	1x USB2 expansion 14-pin header (2x7-pin, 1,27 mm pitch spacing) (1)	JUSB
	1x Modem USB & PCIe interface mini-PICe connector (0,8 mm pitch spacing)	JMODEM
CAN Bus	2x CAN on a 6-pin header (2x3-pin, 2,5 mm pitch spacing)	JCAN
mSATA	1x mSATA & PCIe interface mini-PCIe connector (0,8 mm pitch spacing)	JSATA
Micro-SD	1x Micro-SD card connector	JSD2
SIM connector	1x SIM-card 6-pin type push-push connector	JSIM
UART	4x Serial UART 3V3 expansion 6-pin header (1x6-pin, 2,5 mm pitch spacing)	JSER0, JSER1, JSER2, JSER3
PCI ports	1x PCI expansion 20-pin header (2x10-pin, 1,27 mm pitch spacing)	JPCIE
	2x PCI ports through mini-PCIe connectors (4)	JMODEM, JSATA
SPI	1x SPI 20-pin header (2x10-pin, 1,27 mm pitch spacing)	JSPI
Expansion header	1x I/O Expansion 28-pin header (2x14-pin, 2,54 mm pitch spacing) (5)	JGPIO
Boot Mode	3x Boot jumpers 6-pin header (2x3-pin, 2,54 mm pitch spacing)	JBOOT
Control Signals	1x Control 20-pin header (2x10-pin, 1,27 mm pitch spacing) (6)	JCTL
Button LED	1x Button with Blue and Red LEDs integrated	S1200
RTC Battery	Lithium ion rechargeable battery 3 V / 7 mAh (7)	BT300
Power Supply	Power from expansion connectors: 5 V	J5V
Power Consumption	0.13 A	-
Thermal	Industrial temperature: -40ºC to +80ºC	-
Form Factor	Small SMARC size: 82,00 mm x 50,00 mm	-
	BASE SMARC EXPANSION: 142,00 mm x 90,00 mm	
	Case dimensions: 150,00 mm x 100,00 mm x 30,00 mm	
Humidity	93% relative Humidity at 40 ºC, non-condensing (according to IEC 60068-2-78)	-
MTBF	131400 hours (>15 years)	-

Notes	
(1)	USB2 port to be implemented by User.
(2)	Expansion board is prepared to connect 5" LCD screen with touchscreen of this model directly.
(3)	LCD signals to be used by the User to connect its desired LCD and Touchscreen model.
(4)	JMODEM and JSATA have a double functionality.
(5)	Multiple signals: JGPIO, I2C and Control pins.
(6)	Management pins defined by SMARC standard. Check documentation of your processor module to know what are available.
(7)	Allow to maintain running the Real Time Clock.
(8)	It is needed up to 5 A if all features in the Expansion Board are used at the same time.

Table 2 On-board features

3.4 IGEP™ SMARC BASE EXPANSION COMPONENTS MAP

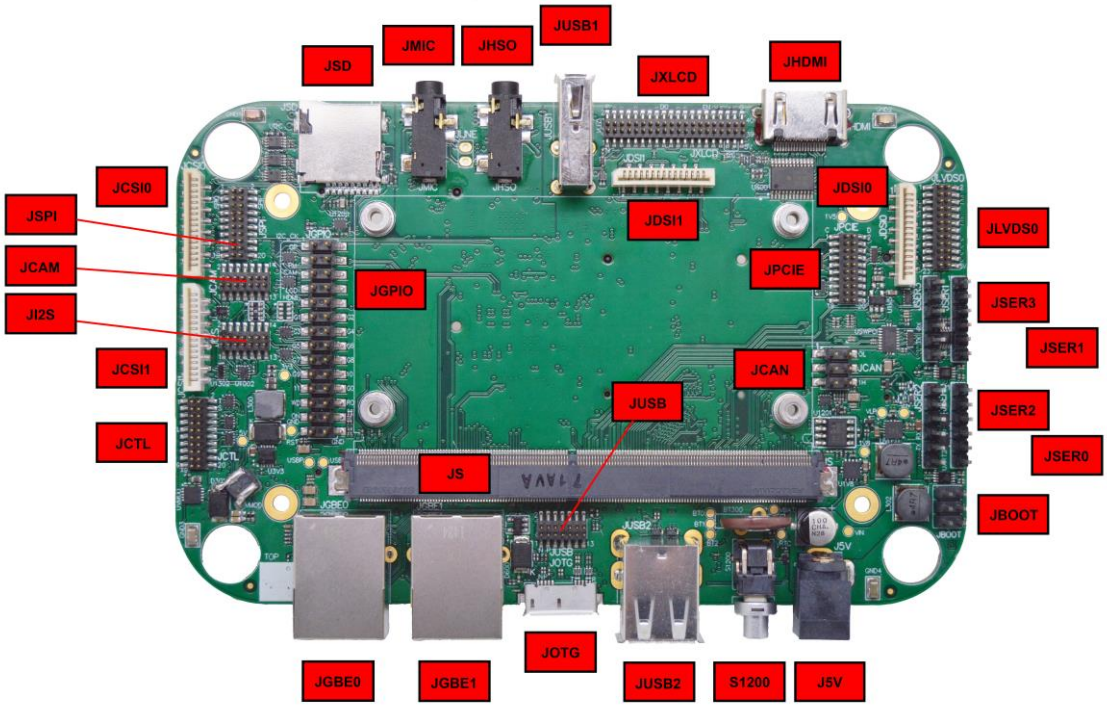


Figure 5 SMARC BASE EXPANSION Components Map – Top view

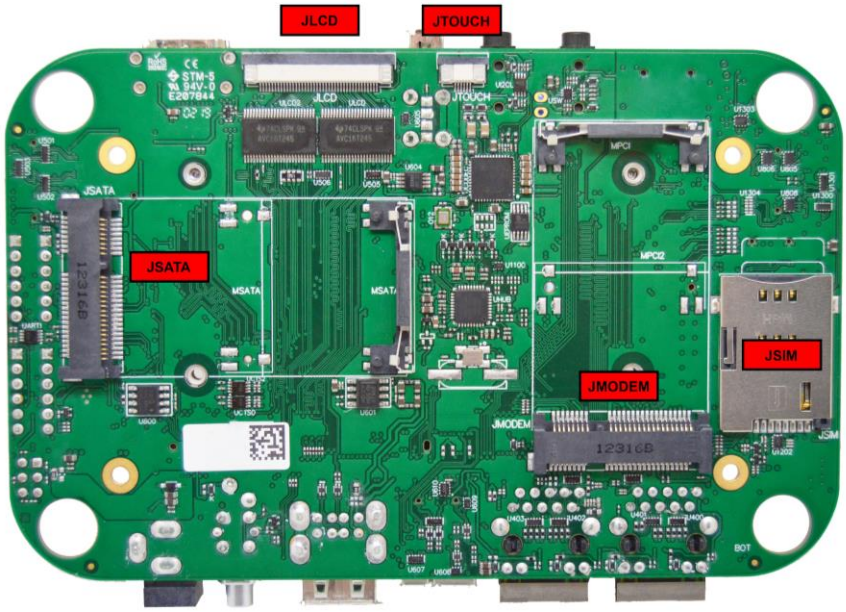


Figure 6 SMARC BASE EXPANSION Components Map – Top view

4 SMARC EXPANSION CONNECTOR INTERFACE

4.1 SMARC INTERFACE DEFINITION

IGEP™ SMARC™ Expansion has a 314-pin SMARC interface (156 on TOP side and 158 on BOTTOM side), providing lots of features which could be used in custom application. The module sizes are 82mm x 50mm as the SMARC standard defines. The module pins are numbered as P1 - P156 (TOP side) and S1 - S158 (BOTTOM side).

Next figure shows the area and pin numbering of the SMARC interface.

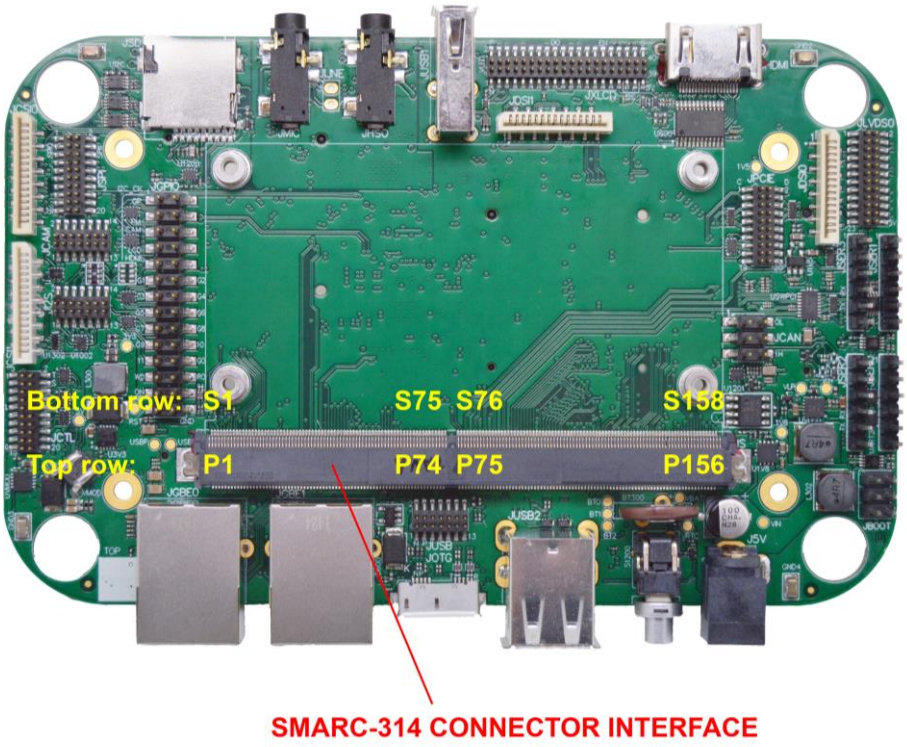


Figure 7 SMARC interface area (TOP Side)

The IGEP™ SMARC BASE EXPANSION permit install modules like a target through this SMARC interface to any of the standard connectors existing on the market. Next table shows some valid references (consult the page 73 on the SMARC 2.1 Specification to find more information).

Manufacturer	Part Number	Height
FOXCONN	AS0B821-S43B-*H	4,3 mm
FOXCONN	AS0B821-S43N-*H	4,3 mm
FOXCONN	AS0B826-S43B-*H	4,3 mm
FOXCONN	AS0B826-S43N-*H	4,3 mm
JAE	MM70-314B2-1-R500	4,3 mm
Aces	91781-314 2 8-001	5,2 mm
FOXCONN	AS0B821-S55B-*H	5,50 mm

FOXCONN	AS0B821-S55N-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B821-S78B-*H	7,80 mm
FOXCONN	AS0B821-S78N-*H	7,80 mm
FOXCONN	AS0B826-S78B-*H	7,80 mm
FOXCONN	AS0B826-S78N-*H	7,80 mm
Yamaichi	CN113-314-2001	7,80 mm

Table 3 Valid SMARC connector part numbers

Developers must consider the SMARC connector height according to their expansion board needs.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards.

4.2 PINOUT TABLE OF SMARC (VERSION) EXPANSION INTERFACE

This chapter contains all the pinout details for the SMARC-314 expansion interface. The table below shows the meaning of each column in table 5, where is collected all the pins and its main functions.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC-314 interface. It is either for Primary Side (Top Side, P#) and Secondary Side (Bottom Side, S#).	
VOLTAGE LEVEL	Signal Level Voltage	
	5V	5 V signal
	3V0	3,0 V signal
	3V3	3,3 V signal
	1V8	1,8 V signal
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface.
	LVDS D-PHY	LVDS signaling used for MIPI CSI camera interfaces.
	TMDS	LVDS signaling used for HDMI display interfaces.
	USB	DC coupled differential signaling used for traditional (non-Super-Speed) USB signals
	USB SS	LVDS signaling used for Super Speed USB 3.0
	PCIE	LVDS signaling used for PCIe interfaces.
	SATA	LVDS signaling used for SATA interfaces.
	GND	Digital ground.
	NC	No connected. This pin should be floating.
TYPE	Indicates pin type.	
	Power	Power signal.
	Input	CMOS input pin.
	Output	CMOS output pin.
	IO	CMOS input and output pin.
	Output OD	Open drain output pin.
	IO OD	Open drain input and output pin.
	NC	No connected. This pin should be floating.
MAIN FUNCTION	Main or suggested function.	
COMMENTS	Clarification for the related SMARC-314 connector pin. See device chapter for more information.	
OTHER FUNCTION	Possible alternate function.	
PDN	Pull-down resistor. If it is needed, in this column appears its value.	
PUP	Pull-up resistor. If it is needed, in this column appears its value.	

Table 4 SMARC expansion interface information

COLORS	INFORMATION
	Power Sources (Supply Voltages)
	Signal Level Voltage (Digital and Analog Ground)
	Control Signals
	Ethernet
	USB connections
	I2C
	SPI
	Wifi/Bluetooth and SD/SD card interface
	UART
	I2S
	CAN bus
	GPIOs
	Analog Inputs
	DVI
	LCD
	CSI - CAM
	RTC Battery

Table 5 Color Leyend

The following table includes all the pins and its description. Please, be careful with the name of pins related to Primary (Top side, pins PXXX) and Secondary (Bottom side, pins SXXX) sides of SMARC connector.

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
Primary (Top) Side							
P1	1V8	Input	PCAM_PXL_CK1	Parallel Camera Pixel Clock 1			
P2	GND	Power	GND	Digital ground			
P3	LVDS D-PHY	Input	CSI1_CK+	CSI differential Clock input.	PCAM_D0		
P4	LVDS D-PHY	Input	CSI1_CK-	CSI differential Clock input.	PCAM_D1		
P5	1V8	Input	PCAM_DE	Parallel Camera Data Enable	GBE1_SDP		
P6	1V8	Output	PCAM_MCK	Parallel Camera Master Clock	GBE0_SDP		
P7	LVDS D-PHY	Input	CSI1_D0+	CSI D0 differential data input.	PCAM_D2		
P8	LVDS D-PHY	Input	CSI1_D0-	CSI D0 differential data input.	PCAM_D3		
P9	GND	Power	GND	Digital ground			
P10	LVDS D-PHY	Input	CSI1_D1+	CSI D1 differential data input.	PCAM_D4		
P11	LVDS D-PHY	Input	CSI1_D1-	CSI D1 differential data input.	PCAM_D5		
P12	GND	Power	GND	Digital ground			
P13	LVDS D-PHY	Input	CSI1_D2+	CSI D2 differential data input.	PCAM_D6		
P14	LVDS D-PHY	Input	CSI1_D2-	CSI D2 differential data input.	PCAM_D7		
P15	GND	Power	GND	Digital ground			
P16	LVDS D-PHY	Input	CSI1_D3+	CSI D3 differential data input.	PCAM_D8		
P17	LVDS D-PHY	Input	CSI1_D3-	CSI D3 differential data input.	PCAM_D9		
P18	GND	Power	GND	Digital ground			
P19	GBE MDI	IO	GBE0_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).			
P20	GBE MDI	IO	GBE0_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).			
P21	3V3	Ouptput OD	GBE0_LINK100#	Link speed indication LED for 100 Mbps. Active low.			
P22	3V3	Ouptput OD	GBE0_LINK1000#	Link speed indication LED for 1000 Mbps. Active low.			
P23	GBE MDI	IO	GBE0_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P24	GBE MDI	IO	GBE0_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).			
P25	3V3	Ouptput OD	GBE0_LINK_ACT#	GB Ethernet Link/Activity indication LED. Active low.			
P26	GBE MDI	IO	GBE0_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).	PHY0_RX-		
P27	GBE MDI	IO	GBE0_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).	PHY0_RX+		
P28	3V3	Output	GBE0_CTREF	Reference voltage for Carrier Board Ethernet magnetic.			
P29	GBE MDI	IO	GBE0_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).	PHY0_TX-		
P30	GBE MDI	IO	GBE0_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).	PHY0_TX+		
P31	1V8	Output	SPI0_CS1#	SPI0 Interface: Master Chip Select 1. Active low.			
P32	GND	Power	GND	Digital ground			
P33	3V3	Input	SD_WP	SD Card Write Protect			10K
P34	3V3	IO	SDIO_CMD	SD card 4-bit Interface: Command Line.			10K
P35	3V3	Input	SDIO_CD#	SD card 4-bit Interface: Card Detect.			10K
P36	3V3	Output	SDIO_CK	SD card 4-bit Interface: Clock.			10K
P37	3V3	Output	SDIO_PWR_EN	SD Power Enable			
P38	GND	Power	GND	Digital ground			
P39	3V3	IO	SDIO_D0	SD card 4-bit Interface: data path (D0).			10K
P40	3V3	IO	SDIO_D1	SD card 4-bit Interface: data path (D1).			10K
P41	3V3	IO	SDIO_D2	SD card 4-bit Interface: data path (D2).			10K
P42	3V3	IO	SDIO_D3	SD card 4-bit Interface: data path (D3).			10K
P43	1V8	Output	SPI0_CS0#	SPI0 Interface: Master Chip Select 0. Active low.			
P44	1V8	Output	SPI0_CK	SPI0 Interface: Clock.			
P45	1V8	Input	SPI0_DIN	SPI0 Interface: Master Data Input.			
P46	1V8	Output	SPI0_DO	SPI0 Interface: Master Data Output.			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P47	GND	Power	GND	Digital ground			
P48	SATA	Output	SATA_TX+	SATA_TX+ Sata Pair TX (3)			
P49	SATA	Output	SATA_TX-	SATA_TX- Sata Pair TX (3)			
P50	GND	Power	GND	Digital ground			
P51	SATA	Output	SATA_RX+	SATA_RX+ Sata Pair RX (3)			
P52	SATA	Output	SATA_RX-	SATA_RX- Sata Pair RX (3)			
P53	GND	Power	GND	Digital ground			
P54	1V8	Output	SPI1_CS0#	SPI1 Interface: Master Chip Select 0. Active low.			
P55	1V8	Output	SPI1_CS1#	SPI1 Interface: Master Chip Select 1. Active low.			
P56	1V8	Output	SPI1_CK	SPI1 Interface: Clock.			
P57	1V8	Input	SPI1_DIN	SPI1 Interface: Master Data Input.	ESPI_IO_0		
P58	1V8	Output	SPI1_DO	SPI1 Interface: Master Data Output.	ESPI_IO_1		
P59	GND	Power	GND	Digital ground			
P60	USB	IO	USB0+	UBS-OTG: USB2.0 differential data input.			
P61	USB	IO	USB0-	UBS-OTG: USB2.0 differential data input.			
P62	3V3	IO OD	USB0_EN_OC#	USB-OTG: Enable (active High)-Overcurrent (active Low) PIN			10K
P63	5V	Input	USB_OTG_VBUS	USB-OTG: USB2.0 Host power detection when this port is used as a device.			
P64	1V8	Input	USB_OTG_ID	USB-OTG: USB2.0 OTG ID input, active high.			
P65	USB	IO	USB1+	UBS1: USB2.0 differential data input. Internally used by HUB-1-2-3-4 (2)	Internally used by HUB		
P66	USB	IO	USB1-	UBS1: USB2.0 differential data input. Internally used by HUB-1-2-3-4 (2)	Internally used by HUB		
P67	3V3	IO OD	USB1_EN_OC#	USB1: Enable OUT(active High)-Overcurrent IN(active Low) PIN			10K
P68	GND	Power	GND	Digital ground			
P69	USB	IO	USB2+	UBS2: USB2.0 differential data input.			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P70	USB	IO	USB2-	UBS2: USB2.0 differential data input.			
P71	3V3	IO OD	USB2_EN_OC#	USB2: Enable OUT(active High)-Overcurrent IN(active Low) PIN			10K
P72	1V8	Input	PCIE_C_PRSNTn	PCIE-C Present (active Low)			
P73	3V3	Input	PCIE_B_PRSNTn	PCIE-B Present (active Low)			10K
P74	3V3	Input	PCIE_A_PRSNTn	PCIE-A Present (active Low)	USB3_EN_OC#		10K
P75	3V3	Output	PCIE_A_RST#	PCIE-A Reset (active Low)			10K
P76	3V3	Input	PCIE_C_CKREQ	PCIE-C Clock Request (active Low)	USB4_EN_OC#		10K
P77	3V3	Input	PCIE_B_CKREQ	PCIE-B Clock Request (active Low)			10K
P78	3V3	Input	PCIE_A_CKREQ	PCIE-A Clock Request (active Low)			10K
P79	GND	Power	GND	Digital ground			
P80	PCIE	Output	PCIE_C_REFCK_P	PCIE-C Reference Clock Pair +			
P81	PCIE	Output	PCIE_C_REFCK_N	PCIE-C Reference Clock Pair -			
P82	GND	Power	GND	Digital ground			
P83	PCIE	Output	PCIE_A_REFCK_P	PCIE-A Reference Clock Pair +			
P84	PCIE	Output	PCIE_A_REFCK_N	PCIE-A Reference Clock Pair -			
P85	GND	Power	GND	Digital ground			
P86	PCIE	Output	PCIE_A_RX_P	PCIE-A Receiver Pair +			
P87	PCIE	Output	PCIE_A_RX_N	PCIE-A Receiver Pair -			
P88	GND	Power	GND	Digital ground			
P89	PCIE	Output	PCIE_A_TX_P	PCIE-A Transmitter Pair +			
P90	PCIE	Output	PCIE_A_TX_N	PCIE-A Transmitter Pair -			
P91	GND	Power	GND	Digital ground			
P92	TMDS	Output	HDMI_D2+	HDMI differential data input D2.			
P93	TMDS	Output	HDMI_D2-	HDMI differential data input D2.			
P94	GND	Power	GND	Digital ground			
P95	TMDS	Output	HDMI_D1+	HDMI differential data input D1.			
P96	TMDS	Output	HDMI_D1-	HDMI differential data input D1.			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P97	GND	Power	GND	Digital ground			
P98	TMDS	Output	HDMI_D0+	HDMI differential data input D0.			
P99	TMDS	Output	HDMI_D0-	HDMI differential data input D0.			
P100	GND	Power	GND	Digital ground			
P101	TMDS	Output	HDMI_CK+	HDMI differential clock output pair.			
P102	TMDS	Output	HDMI_CK-	HDMI differential clock output pair.			
P103	GND	Power	GND	Digital ground			
P104	1V8	Input	HDMI_HPD	HDMI Hot Plug detect input. (1)			
P105	1V8	Output OD	HDMI_CTRL_CK	I2C Clock line dedicated to HDMI. Connected to I2C2_CLK (1)			
P106	1V8	IO OD	HDMI_CTRL_DAT	I2C Data line dedicated to HDMI. Connected to I2C2_SDA (1)			
P107	1V8	IO	HDMI_CEC	HDMI Consumer Electronic Control (1)			
P108	1V8	IO	GPIO0	General Purpose Input Output / CAM0 Power (1)			
P109	1V8	IO	GPIO1	General Purpose Input Output / CAM1 Power (Internal Enable-1 USB; Active High) (1)	(Internal Enable-1 USB)		
P110	1V8	IO	GPIO2	General Purpose Input Output / CAM0 Reset (Internal Enable-2 USB; Active High) (1)	(Internal Enable-2 USB)		
P111	1V8	IO	GPIO3	General Purpose Input Output / CAM1 Reset (Internal Enable-3 USB; Active High) (1)	(Internal Enable-3 USB)		
P112	1V8	IO	GPIO4	General Purpose Input Output (Internal Reset CODEC; Active Low)	(Internal Reset CODEC)		
P113	1V8	IO	GPIO5-PWM1	General Purpose Input Output / PWM1			
P114	1V8	IO	GPIO6	General Purpose Input Output (Internal Reset MODEM; Active High) (1)	(Internal Reset MODEM)		
P115	1V8	IO	GPIO7	General Purpose Input Output (Internal SATA-PCIE_B Selection; Active High) (1)	(Internal SATA-PCIE_B)		
P116	1V8	IO	GPIO8	General Purpose Input Output (Internal SATA & MODEM LED W; Active High) (1)	(Internal SATA & MODEM)		

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P117	1V8	IO	GPIO9	General Purpose Input Output (Internal USER_BUTTON, Active Low)	(Internal USER_BUTTON)		
P118	1V8	IO	GPIO10	General Purpose Input Output (Internal DSI1_EN & USER_LED_BLUE; Active High) (1)	(Internal DSI1_EN & USER_LED_BLUE)		
P119	1V8	IO	GPIO11	General Purpose Input Output (USER_LED_RED; Active High) (1)	(Internal USER_LED_RED)		
P120	GND	Power	GND	Digital ground			
P121	1V8	IO OD	I2C_PM_CK	I2C2: Clock signal. Shared with internal EEPROM	(Internal EEPROM)		
P122	1V8	IO OD	I2C_PM_DAT	I2C2: Data signal. Shared with internal EEPROM	(Internal EEPROM)		
P123	1V8	Input	BOOT_SEL0#	Boot device. Active low.			
P124	1V8	Input	BOOT_SEL1#	Boot device. Active low.			
P125	1V8	Input	BOOT_SEL2#	Boot device. Active low.			
P126	1V8	Output	RESET_OUT#	General purpose reset output to Carrier. (Internal RESET HUB; Active High) (1)	(Internal RESET HUB)		
P127	1V8	Input	RESET_IN#	Reset input from Carrier board. Active low.			
P128	1V8	Input	POWER_BTN#	Power button input from Carrier board. Active low.			
P129	1V8	Output	SER0_TX	SERIAL-0: Asynchronous serial port 4 data out. (1)			
P130	1V8	Input	SER0_RX	SERIAL-0: Asynchronous serial port 4 data in. (1)			
P131	1V8	Output	SER0_RTS#	SERIAL-0: Request to Send handshake line. Active low. (1)			
P132	1V8	Input	SER0_CTS#	SERIAL-0: Clear to Send handshake line. Active low. (1)			
P133	GND	Power	GND	Digital ground			
P134	1V8	Output	SER1_TX	SERIAL-1: Asynchronous serial port 4 data out. (1)			
P135	1V8	Input	SER1_RX	SERIAL-1: Asynchronous serial port 4 data in. (1)			
P136	1V8	Output	SER2_TX	SERIAL-2: Asynchronous serial port 4 data out. (1)			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
P137	1V8	Input	SER2_RX	SERIAL-2: Asynchronous serial port 4 data in. (1)			
P138	1V8	Output	SER2_RTS#	SERIAL-2: Request to Send handshake line. Active low. (1)			
P139	1V8	Input	SER2_CTS#	SERIAL-2: Clear to Send handshake line. Active low. (1)			
P140	1V8	Output	SER3_TX	SERIAL-3: Asynchronous serial port 4 data out. (1)			
P141	1V8	Input	SER3_RX	SERIAL-3: Asynchronous serial port 4 data in. (1)			
P142	GND	Power	GND	Digital ground			
P143	1V8	Output	CAN0_TX	CAN0 Transmitter Line (1)			
P144	1V8	Input	CAN0_RX	CAN0 Receiver Line (1)			
P145	1V8	Output	CAN1_TX	CAN1 Transmitter Line (1)			
P146	1V8	Input	CAN1_RX	CAN1 Receiver Line (1)			
P147	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P148	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P149	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P150	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P151	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P152	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P153	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P154	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P155	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
P156	5V	Power	VDD_IN	Pins used to power up the module. 4,75 V to 5,25 V			
Secondary (Bottom) Side							
S1	1V8	IO OD	I2C_CAM1_CK	I2C2: Clock signal. Shared with I2C_CAM_CK (1)	PCAM_VSYNC		

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S2	1V8	IO OD	I2C_CAM1_DAT	I2C2: Data signal. Shared with I2C_CAM_DAT (1)	PCAM_HSYNC		
S3	GND	Power	GND	Digital ground			
S4	1V8	Output	PCAM_PXL_CK0	Parallel Camera Pixel Clock 0			
S5	1V8	IO OD	I2C_CAM_CK	I2C2: Clock signal. Shared with I2C_CAM1_CK (1)			
S6	1V8	Output	CAM_MCK	Camera Master Clock			
S7	1V8	IO OD	I2C_CAM_DAT	I2C2: Data signal. Shared with I2C_CAM1_DAT (1)			
S8	LVDS D-PHY	Input	CSI0_CK+	CSI differential Clock input.	PCAM_D10		
S9	LVDS D-PHY	Input	CSI0_CK-	CSI differential Clock input.	PCAM_D11		
S10	GND	Power	GND	Digital ground			
S11	LVDS D-PHY	Input	CSI0_D0+	CSI D0 differential data input.	PCAM_D12		
S12	LVDS D-PHY	Input	CSI0_D0-	CSI D0 differential data input.	PCAM_D13		
S13	GND	Power	GND	Digital ground			
S14	LVDS D-PHY	Input	CSI0_D1+	CSI D1 differential data input.	PCAM_D14		
S15	LVDS D-PHY	Input	CSI0_D1-	CSI D1 differential data input.	PCAM_D15		
S16	GND	Power	GND	Digital ground			
S17	GBE MDI	IO	GBE1_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).			
S18	GBE MDI	IO	GBE1_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).			
S19	3V3	Ouptput OD	GBE1_LINK100	GB Ethernet Link speed indication LED for 100 Mbps. Active low.			
S20	GBE MDI	IO	GBE1_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).			
S21	GBE MDI	IO	GBE1_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).			
S22	3V3	Ouptput OD	GBE1_LINK1000#	Link speed indication LED for 1000 Mbps. Active low.			
S23	GBE MDI	IO	GBE1_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).			
S247	GBE MDI	IO	GBE1_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).			
S25	GND	Power	GND	Digital ground			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S26	GBE MDI	IO	GBE1_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).			
S27	GBE MDI	IO	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).			
S28	3V3	Power	GBE1_CTREF	Reference voltage for Carrier Board Ethernet magnetic.			
S29	PCIE	Output	PCIE_D_TX_P	PCIE-D Transmitter Pair +			
S30	PCIE	Output	PCIE_D_TX_N	PCIE-D Transmitter Pair -			
S31	3V3	Ouptput OD	GBE1_LINK_ACT#	GB Ethernet Link/Activity indication LED. Active low.			
S32	PCIE	Output	PCIE_D_RX_P	PCIE-D Receiver Pair +			
S33	PCIE	Output	PCIE_D_RX_N	PCIE-D Receiver Pair -			
S34	GND	Power	GND	Digital ground			
S35	NC	NC	Not connected	Not connected	USB4_P		
S36	NC	NC	Not connected	Not connected	USB4_N		
S37	5V	Input	USB3_VBUS_DET	USB-3: USB2.0 Host power detection when this port is used as a device.			
S38	1V8	Output	AUDIO_MCK	Audio Digital Master Clock. Used internally by CODEC.	(Internal CODEC)		
S39	1V8	IO	I2S0_SYNC	I2S0 Left & Right Audio synchronization clock. Used internally by CODEC.	(Internal CODEC)		
S40	1V8	Output	I2S0_SDOUT	I2S0 Digital Audio output. Used internally by CODEC.	(Internal CODEC)		
S41	1V8	Input	I2S0_SDIN	I2S0 Digital Audio input. Used internally by CODEC.	(Internal CODEC)		
S42	1V8	IO	I2S0_CK	I2S0 Digital Audio BIT clock. Used internally by CODEC.	(Internal CODEC)		
S43	1V8	IO	I2S1_SYNC	I2S1 Left & Right Audio synchronization clock.	ESPI_ALERT0		
S44	1V8	Output	I2S1_SDOUT	I2S1 Digital Audio output.	ESPI_ALERT1		
S45	1V8	Input	I2S1_SDIN	I2S1 Digital Audio input.			
S46	1V8	IO	I2S1_CK	I2S1 Digital Audio BIT clock.			
S47	GND	Power	GND	Digital ground			
S48	1V8	IO OD	I2C_GP_CK	I2C General Purpose: Clock signal. Shared internally with CODEC	(Internal CODEC)		

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S49	1V8	IO OD	I2C_GP_DAT	I2C General Purpose: Data signal. Shared internally with CODEC	(Internal CODEC)		
S50	1V8	IO	I2S2_SYNC	I2S2 Left & Right Audio synchronization clock.			
S51	1V8	Output	I2S2_SDOUT	I2S2 Digital Audio output.			
S52	1V8	Input	I2S2_SDIN	I2S2 Digital Audio input.			
S53	1V8	IO	I2S2_CK	I2S2 Digital Audio BIT clock.			
S54	1V8	IO	SATA_ACT	SATA ACTIVITY			
S55	3V3	IO OD	USB5_EN_OC#	USB-5: Enable (active High)-Overcurrent (active Low) PIN			
S56	1V8	IO	ESPI_IO_2	ESPI Input-Output Data 2			
S57	1V8	IO	ESPI_IO_3	ESPI Input-Output Data 3			
S58	1V8	Output	ESPI_RESET#	ESPI Reset; Active Low			
S59	USB	IO	USB5+	UBS5: USB2.0 differential data input.	SPDIF_OUT		
S60	USB	IO	USB5-	UBS5: USB2.0 differential data input.	SPDIF_IN		
S61	GND	Power	GND	Digital ground			
S62	USB SS	Output	USB3_SSTX+	USB3 SS: TX differential pair.			
S63	USB SS	Output	USB3_SSTX-	USB3 SS: TX differential pair.			
S64	GND	Power	GND	Digital ground			
S65	USB SS	Input	USB3_SSRX+	USB1 SS: RX differential pair.			
S66	USB SS	Input	USB3_SSRX-	USB1 SS: RX differential pair.			
S67	GND	Power	GND	Digital ground			
S68	USB	IO	USB3+	UBS3: USB2.0 differential data input.			
S69	USB	IO	USB3-	UBS3: USB2.0 differential data input.			
S70	GND	Power	GND	Digital ground			
S71	USB SS	Output	USB2_SSTX+	USB2 SS: TX differential pair.			
S72	USB SS	Output	USB2_SSTX-	USB2 SS: TX differential pair.			
S73	GND	Power	GND	Digital ground			
S74	USB SS	Input	USB2_SSRX+	USB2 SS: RX differential pair.			
S75	USB SS	Input	USB2_SSRX-	USB2 SS: RX differential pair.			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S76	3V3	Output	PCIE_B_RST#	PCIE-B Reset (active Low)			
S77	3V3	Output	PCIE_C_RST#	PCIE-C Reset (active Low)			
S78	PCIE	Output	PCIE_C_RX_P	PCIE-C Receiver Pair +			
S79	PCIE	Output	PCIE_C_RX_N	PCIE-C Receiver Pair -			
S80	GND	Power	GND	Digital ground			
S81	PCIE	Output	PCIE_C_TX_P	PCIE-C Transmitter Pair +			
S82	PCIE	Output	PCIE_C_TX_N	PCIE-C Transmitter Pair -			
S83	GND	Power	GND	Digital ground			
S84	PCIE	Output	PCIE_B_REFCK_P	PCIE-B Reference Clock Pair +			
S85	PCIE	Output	PCIE_B_REFCK_N	PCIE-B Reference Clock Pair -			
S86	GND	Power	GND	Digital ground			
S87	PCIE	Output	PCIE_B_RX_P	PCIE-B Receiver Pair + (3)			
S88	PCIE	Output	PCIE_B_RX_N	PCIE-B Receiver Pair - (3)			
S89	GND	Power	GND	Digital ground			
S90	PCIE	Output	PCIE_B_TX_P	PCIE-B Transmitter Pair + (3)			
S91	PCIE	Output	PCIE_B_TX_N	PCIE-B Transmitter Pair - (3)			
S92	GND	Power	GND	Digital ground			
S93	1V8	Output	LCD_D0	DiSPLAY DATA BIT (1)			
S94	1V8	Output	LCD_D1	DiSPLAY DATA BIT (1)			
S95	1V8	Output	LCD_D2	DiSPLAY DATA BIT (1)			
S96	1V8	Output	LCD_D3	DiSPLAY DATA BIT (1)			
S97	1V8	Output	LCD_D4	DiSPLAY DATA BIT (1)			
S98	1V8	Output	LCD_D5	DiSPLAY DATA BIT (1)			
S99	1V8	Output	LCD_D6	DiSPLAY DATA BIT (1)			
S100	1V8	Output	LCD_D7	DiSPLAY DATA BIT (1)			
S101	GND	Power	GND	Digital ground			
S102	1V8	Output	LCD_D8	DiSPLAY DATA BIT (1)			
S103	1V8	Output	LCD_D9	DiSPLAY DATA BIT (1)			
S104	1V8	Output	LCD_D10	DiSPLAY DATA BIT (1)	USB3_OTG_ID		

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S105	1V8	Output	LCD_D11	DiSPLAY DATA BIT (1)			
S106	1V8	Output	LCD_D12	DiSPLAY DATA BIT (1)			
S107	1V8	Output	LCD_D13	DiSPLAY DATA BIT (1)			
S108	1V8	Output	LCD_D14	DiSPLAY DATA BIT (1)	DSI1 X+		
S109	1V8	Output	LCD_D15	DiSPLAY DATA BIT (1)	DSI1 X-		
S110	GND	Power	GND	Digital ground			
S111	1V8	Output	LCD_D16	DiSPLAY DATA BIT (1)	DSI1 0+		
S112	1V8	Output	LCD_D17	DiSPLAY DATA BIT (1)	DSI1 0-		
S113	1V8	Output	LCD_D18	DiSPLAY DATA BIT (1)			
S114	1V8	Output	LCD_D19	DiSPLAY DATA BIT (1)	DSI1 1+		
S115	1V8	Output	LCD_D20	DiSPLAY DATA BIT (1)	DSI1 1-		
S116	1V8	Output	LCD_D21	DiSPLAY DATA BIT (1)			
S117	1V8	Output	LCD_D22	DiSPLAY DATA BIT (1)	DSI1 2+		
S118	1V8	Output	LCD_D23	DiSPLAY DATA BIT (1)	DSI1 2-		
S119	GND	Power	GND	Digital ground			
S120	1V8	Output	LCD_DE	DISPLAY DATA READY (1)	DSI1 3+		
S121	1V8	Output	LCD_VS	DISPLAY VERTICAL SYNCHRONISM (1)	DSI1 3-		
S122	1V8	Output	LCD_HS	DISPLAY HORIZONTAL SYNCHRONISM (1)			
S123	1V8	Output	LCD_PCK	DISPLAY PIXEL CLOCK (1)			
S124	GND	Power	GND	Digital ground			
S125	LVDS D-PHY	Output	DSI0_D0+	DSI: Data pair 0.	LVDS0_0+		
S126	LVDS D-PHY	Output	DSI0_D0-	DSI: Data pair 0.	LVDS0_0-		
S127	1V8	Output	LCD_BKLT_EN	LCD Panel Backlite Enable (1)			
S128	LVDS D-PHY	Output	DSI0_D1+	DSI: Data pair 1.	LVDS0_1+		
S129	LVDS D-PHY	Output	DSI0_D1-	DSI: Data pair 1.	LVDS0_1-		
S130	GND	Power	GND	Digital ground			
S131	LVDS D-PHY	Output	LVDS0_2+	LVDS0: Data pair 2			
S132	LVDS D-PHY	Output	LVDS0_2-	LVDS0: Data pair 2			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S133	1V8	Output	LCD_VDD_EN	GPIO4[20] LCD Panel Power Enable. Internally used by LCD regulator (Active Low) (1)	(Internal LCD REGULATOR)		
S134	LVDS D-PHY	Output	DSI0_CLK+	DSI: Clock pair.	LVDS0_CK+		
S135	LVDS D-PHY	Output	DSI0_CLK-	DSI: Clock pair.	LVDS0_CK-		
S136	GND	Power	GND	Digital ground			
S137	LVDS D-PHY	Output	LVDS0_3+	LVDS0: Data pair 3			
S138	LVDS D-PHY	Output	LVDS0_3-	LVDS0: Data pair 3			
S139	1V8	IO OD	I2C_LCD_CK	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI			
S140	1V8	IO OD	I2C_LCD_DAT	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI			
S141	1V8	IO	LCD_BKLT_PWM	PWM signal for LCD Panel Backlite. Internally used by LCD regulator (1)	(Internal LCD REGULATOR)		
S142	NC	NC	RESERVED	Not connected			
S143	GND	Power	GND	Digital ground			
S144	NC	NC	RESERVED	Not connected	EDP_HPD		
S145	1V8	Output	WDT_TIME_OUT	Watch-Dog-Timer Output			
S146	3V3	Input	PCIE_WAKE#	PCIe wake up interrupt to host			10K
S147	3V0	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal	(Internal Battery Coin Cell)		
S148	1V8	Input	LID#	Lid open/close indication to Module. Low indicates lid closure			
S149	1V8	Input	SLEEP#	Sleep indicator from Carrier board			
S150	1V8	Input	VIN_PWR_BAD#	Power bad indication from Carrier board			
S151	1V8	Input	CHARGING#	Held low by Carrier during battery charging			
S152	1V8	Input	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present			
S153	1V8	Output	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state			
S154	1V8	Output	CARRIER_PWRON#	Carrier board circuits should not be powered up until the Module asserts this signal			

Pin	Volt Level	Type	Main Function	Comments	Other Function	PDN	PUP
S155	1V8	Input	FORCE_RECOV#	Low allows non-protected segments of Module boot device to be rewritten			
S156	1V8	Input	BATLOW#	Battery low indication to Module			
S157	1V8	Input	TEST#	Held low by Carrier to invoke Module vendor specific test function			
S158	GND	Power	GND	Digital ground			

Notes	
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.
(2)	USB HUB internal.
(3)	GPIO7=1 ➔ SEL=0 ➔ PCIE-B; GPIO7=0 ➔ SEL=1 ➔ SATA

Table 6 SMARC pinout description

5 PRODUCT SPECIFICATION SUMMARY

5.1 POWER SOURCES

5.1.1 Supply Voltage

SMARC BASE EXPANSION must be powered by +5 V_{DC} power source and 5 A_{DC} intensity if users wish to expand all board functionalities at the same time. For more information see electrical characteristics table in Chapter 6 ELECTRICAL CHARACTERISTICS.

Power supply input is made through J5V connector. Next figures show the schematic design and the connector location on the Base:

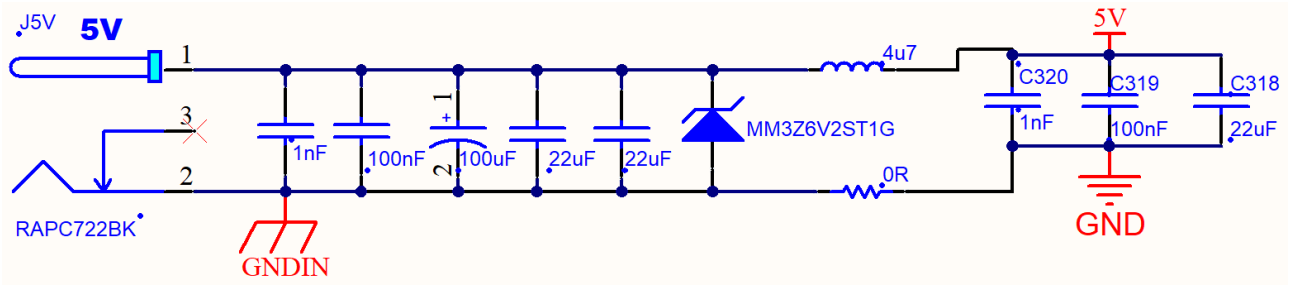


Figure 8 Power Supply Input Schematic

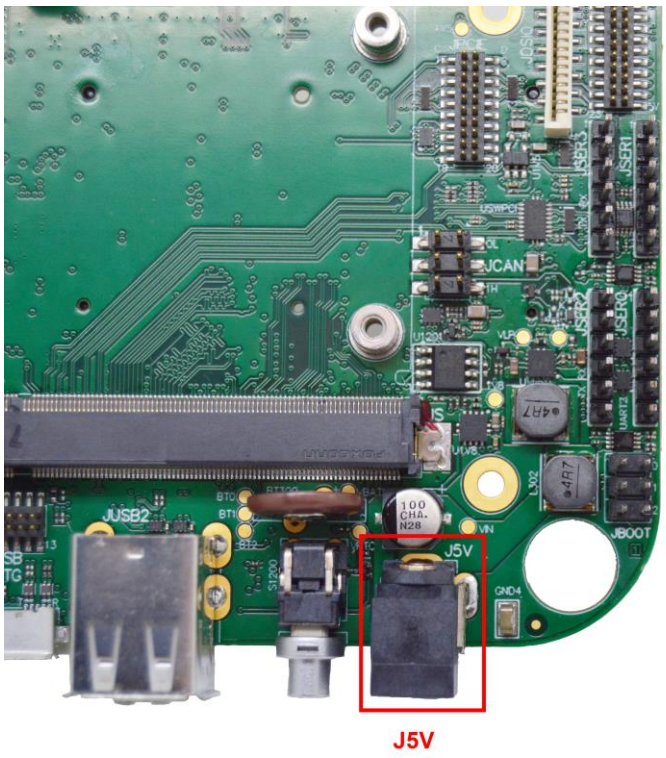


Figure 9 Power Supply Connector (J5V) Location

In the following table there is a summary of all Power Supply pins available related to the MXM3 SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
5V Input Power				
P147	5V	Power	VDD_IN0	Pins powered by +5 V_{DC} power source
P148	5V	Power	VDD_IN1	Pins powered by +5 V_{DC} power source
P149	5V	Power	VDD_IN2	Pins powered by +5 V_{DC} power source
P150	5V	Power	VDD_IN3	Pins powered by +5 V_{DC} power source
P151	5V	Power	VDD_IN4	Pins powered by +5 V_{DC} power source
P152	5V	Power	VDD_IN5	Pins powered by +5 V_{DC} power source
P153	5V	Power	VDD_IN6	Pins powered by +5 V_{DC} power source
P154	5V	Power	VDD_IN7	Pins powered by +5 V_{DC} power source
P155	5V	Power	VDD_IN8	Pins powered by +5 V_{DC} power source
P156	5V	Power	VDD_IN9	Pins powered by +5 V_{DC} power source

Table 7 Power Supply pins

5.1.2 Digital Ground

All the digital GND pins are internally connected. However, the user has to considerer how many of them should connect according to the total consumption of the complete circuit. At the same time, to make easier the buses routing, the GND connection chosen should be the nearest to the function used.

It shall be a minimum of 4 GND pins connected, distributed in the most possible equal way along the MXM3 SMARC connector, to get an equalized ground.

In the following table there is a summary of all GND pins available related to the MXM3 SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Digital Ground				
P2	GND	Power	GND	Digital ground
P9	GND	Power	GND1	Digital ground
P12	GND	Power	GND2	Digital ground
P15	GND	Power	GND3	Digital ground
P18	GND	Power	GND4	Digital ground
P32	GND	Power	GND5	Digital ground
P38	GND	Power	GND6	Digital ground
P47	GND	Power	GND7	Digital ground
P50	GND	Power	GND8	Digital ground
P53	GND	Power	GND9	Digital ground
P59	GND	Power	GND10	Digital ground
P68	GND	Power	GND11	Digital ground
P79	GND	Power	GND34	Digital ground
P82	GND	Power	GND33	Digital ground
P85	GND	Power	GND32	Digital ground
P88	GND	Power	GND31	Digital ground
P91	GND	Power	GND30	Digital ground
P94	GND	Power	GND29	Digital ground
P97	GND	Power	GND28	Digital ground
P100	GND	Power	GND27	Digital ground
P103	GND	Power	GND26	Digital ground

P120	GND	Power	GND25	Digital ground
P133	GND	Power	GND24	Digital ground
P142	GND	Power	GND23	Digital ground
S3	GND	Power	GND12	Digital ground
S10	GND	Power	GND13	Digital ground
S13	GND	Power	GND14	Digital ground
S16	GND	Power	GND15	Digital ground
S25	GND	Power	GND25	Digital ground
S34	GND	Power	GND17	Digital ground
S47	GND	Power	GND18	Digital ground
S61	GND	Power	GND19	Digital ground
S64	GND	Power	GND47	Digital ground
S67	GND	Power	GND20	Digital ground
S70	GND	Power	GND21	Digital ground
S73	GND	Power	GND22	Digital ground
S80	GND	Power	GND46	Digital ground
S83	GND	Power	GND45	Digital ground
S86	GND	Power	GND44	Digital ground
S89	GND	Power	GND43	Digital ground
S92	GND	Power	GND42	Digital ground
S101	GND	Power	GND41	Digital ground
S110	GND	Power	GND40	Digital ground
S119	GND	Power	GND39	Digital ground
S124	GND	Power	GND38	Digital ground
S130	GND	Power	GND37	Digital ground
S136	GND	Power	GND36	Digital ground
S143	GND	Power	GND35	Digital ground
S158	GND	Power	GND	Digital ground

Table 8 Digital Ground pins

5.2 CONTROL SIGNALS

There are different pins used as general control signals. They are related to Boot Mode, Reset functions, the use of an External Pushbutton and some pins related with the Module State Pins.

5.2.1 Boot Modes

There are three pins in the MXM3 SMARC connector which can be used to fix the boot mode of the module (pins 123 to 125 on Top side). They are active low. With them is possible to fix from which device will boot up the module. Next table offers all possible ways.

BOOT2 (P125)	BOOT1 (P124)	BOOT0 (P123)	BOOT MODE
0	0	0	Carrier SATA
0	0	1	Carrier SD Card
0	1	0	Carrier eSPI (CS0#)
0	1	1	Carrier SPI (CS0#)
1	0	0	Module device (NAND, NOR)
1	0	1	Remote boot (Network (GBE) or Serial)
1	1	0	Module eMMC Flash
1	1	1	Module SPI

Table 9 Boot Mode pins

Please, be careful that Some IGEP™ SMARC family boards may not support all options, refer to the module documentation.

Next figures show the schematic design and the connector location on the Base:

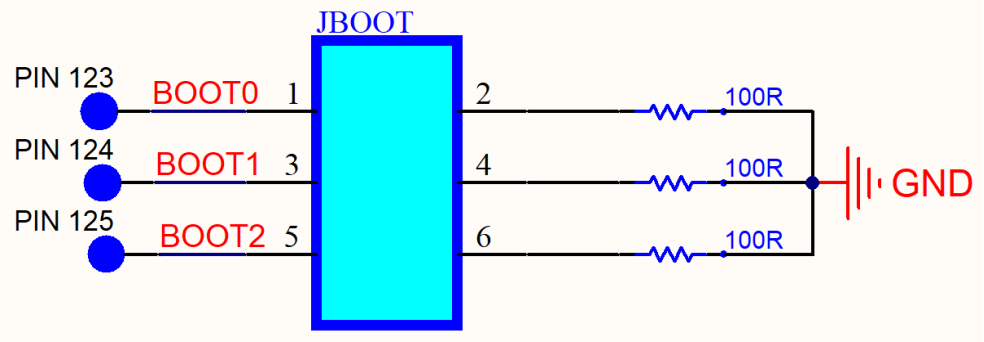


Figure 10 Boot Select Schematic

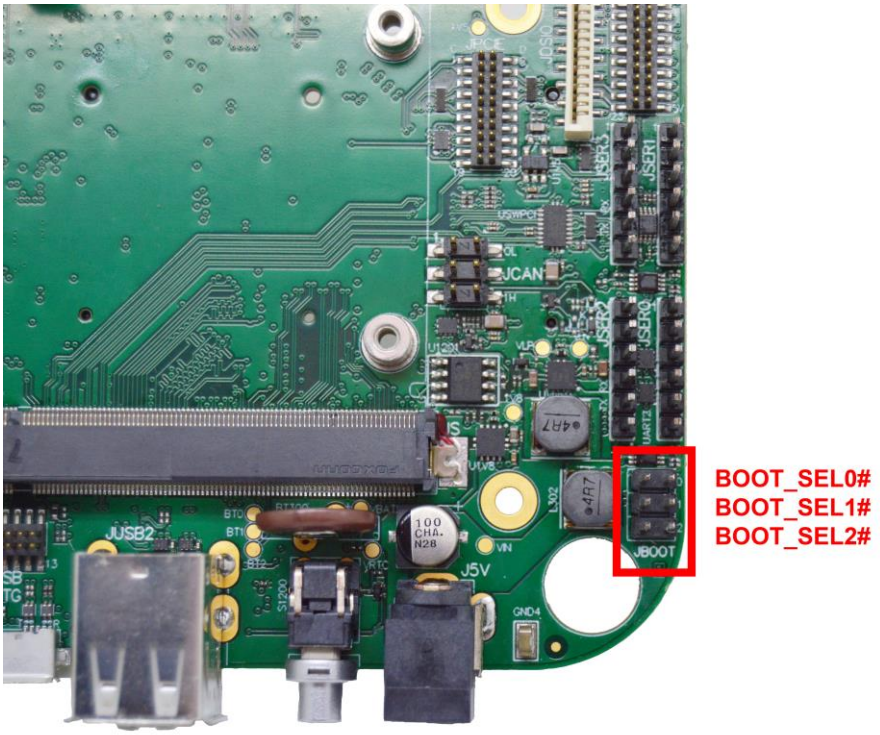


Figure 11 BOOT Connector (JBOOT) Location

5.2.2 Reset pins

There are also two different Reset-IO possibilities. The first one is a General Reset RESET_OUT# (P126) and the other one is a RESET_IN# (P127).

Pin RESET_OUT# (P126) is general purpose reset output to Carrier Board. Related to JGPIO connector (pin 24) and USB HUB (pin 26) (HUB2_RST).

Pin RESET_IN# (P127) is a Reset input from Carrier Board. Related to JGPIO connector (pin 27).

5.2.3 External Pushbutton

Pin POWER_BTN# (P128) is to be used as Power-button input from Carrier Board. This is active low. Related to JGPIO connector (pin 26).

5.2.4 Module State Pins

- **Watchdog Timer output**

Pin WDT_TIME_OUT# (S145) Watchdog interrupt output. This is active low. Related to JGPIO connector (pin 23).

- **Sleep**

Pin SLEEPN# (S149) - Carrier drives to float the line in in-activate state. Active low, level sensitive. Related to JCTL connector (pin 4).

- **Carrier Standby**

Pin CARRIER_STBY# (S153) - The Module shall drive this signal low when the system is in a standby power state. Related to JCTL connector (pin 8).

- **Carrier Power On**

Pin CARRIER_PWR_ON# (S154) - Carrier board circuits (apart from power management and power path circuits) should not be powered until the Module asserts this signal. Related to JGPIO connector (pin 25).

- **Force Recovery**

Pin FORCE_RECOV# (S155) - Low on this pin allows non-protected segments of Module boot device to be rewritten/restored from an external USB Host on Module USB0. Related to JCTL connector (pin 6).

- **Test**

Pin TEST# (S157) - Held low by Carrier to invoke Module vendor specific test function. Related to JCTL connector (pin 2).

The table below shows a summary of all control signals:

Pin	Volt Level	Type	Main Function	Comments
Boot Modes				
P123	1V8	I OD CMOS	BOOT_SEL0#	Input straps determine the module boot device. Active low.
P124	1V8	I OD CMOS	BOOT_SEL1#	Input straps determine the module boot device. Active low.
P125	1V8	I OD CMOS	BOOT_SEL2#	Input straps determine the module boot device. Active low.
Reset functions				
P126	1V8	O CMOS	RESET_OUT#	Pin RESET_OUT# (P126) is general purpose reset output to Carrier Board. Related to JGPIO connector (pin 24) and USB HUB (pin 26) (HUB2_RST).
P127	1V8	I OD CMOS	RESET_IN#	Reset input from Carrier board. Active low. Related to JGPIO connector (pin 27).
External pushbutton				
P128	1V8	I OD CMOS	POWER_BTN#	Power button input from carrier board. Active low. Related to JGPIO connector (pin 26).

State pins				
S145	1V8	O CMOS	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active. Related to JGPIO connector (pin 23).
S149	1V8	I OD CMOS	SLEEP#	Sleep indicator from Carrier Board. Related to JCTL connector (pin 4).
S153	1V8	O CMOS	CARRIER_STBY#	Standby state. Related to JCTL connector (pin 8).
S154	1V8	O CMOS	CARRIER_PWR_ON#	Signal to enable Carrier Board power on. Related to JGPIO connector (pin 25).
S155	1V8	I OD CMOS	FORCE_RECOV#	Force Recovery. Related to JCTL connector (pin 6).
S157	1V8	I OD CMOS	TEST#	Test. Related to JCTL connector (pin 2).

Table 10 Control Signals pins

5.3 ETHERNET

The BASE SMARC EXPANSION includes two RJ45 connectors (JGBE0 and JGBE1), provided for the Ethernet Auto-MDIX Full Duplex 10/100/1000 Base T interface. Both ports are supported by Ethernet Physical Layer Transceivers (PHY) included into the IGEP™ SMARC family processor boards. The expansion board only makes a direct link with the Ethernet port.

The module implements respective physical layers for each interface and a block of pins of SMARC-314 interface that can be connected directly to the Ethernet connectors. Both transmission and reception lines (TX and RX) are differential (there are a total of four pairs for etch Ethernet, and in the pin functions is indicated the Negative and Positive) and they should be connected to magnetics for isolation. The data lines must be equal length and symmetric and respect a 100 Ω differential impedance in the layout traces. The differential pairs must be isolated.

Moreover, the magnetics module has a critical effect, so it must be designed carefully. In order to obtain a smaller size, it is usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they must respect a separation under of 25 mm between them and the RJ45 connector, and 20 mm or greater between them and the SMARC-314 connector.

There is also possible to connect two LEDs. They are used to indicate the good functioning of the Ethernet connection. The first one (GBE0_LINK_ACT# and GBE1_LINK_ACT#) indicates the line activity (LED on indicates a valid link; LED blinking when there is data traffic). The second one (GBE0_LINK100# and GBE1_LINK100#)) is a link speed indication for 100 Mbps. These are usually in green and yellow color.

The last used pins are GBE0_CTREF and GBE1_CTREF. There are to be used as reference voltage for Carrier Board Ethernet magnetic (if it is required by the module GBE PHY).

The following table presents all the Ethernet 10/100/1000 Mbps pins:

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JGBE0					
1	3V3	O CMOS	GBE0_CTREF	P28	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
2	GBE MDI	I/O CMOS	GBE0_MDI0+	P30	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
3	GBE MDI	I/O CMOS	GBE0_MDI0-	P29	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
4	GBE MDI	I/O CMOS	GBE0_MDI1+	P27	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
5	GBE MDI	I/O CMOS	GBE0_MDI1-	P26	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
6	GBE MDI	I/O CMOS	GBE0_MDI2+	P24	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
7	GBE MDI	I/O CMOS	GBE0_MDI2-	P23	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
8	GBE MDI	I/O CMOS	GBE0_MDI3+	P20	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
9	GBE MDI	I/O CMOS	GBE0_MDI3-	P19	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
10	GND	Power	GND	P32	Digital ground
11	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
12	3V3	O OD CMOS	GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity
13	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
14	3V3	O OD CMOS	GBE0_LINK100#	P21	Link speed indication LED for 100 Mbps. Active low.
15	GND	Power	GND	P38	Digital ground
16	GND	Power	GND	P47	Digital ground
JGBE1					
1	3V3	O CMOS	GBE1_CTREF	S28	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
2	GBE MDI	I/O CMOS	GBE1_MDI0+	S17	GB Ethernet pair 0 to magnetics (Media Dependent Interface).

3	GBE MDI	I/O CMOS	GBE1_MDI0-	S18	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
4	GBE MDI	I/O CMOS	GBE1_MDI1+	S20	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
5	GBE MDI	I/O CMOS	GBE1_MDI1-	S21	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
6	GBE MDI	I/O CMOS	GBE1_MDI2+	S23	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
7	GBE MDI	I/O CMOS	GBE1_MDI2-	S247	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
8	GBE MDI	I/O CMOS	GBE1_MDI3+	S26	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
9	GBE MDI	I/O CMOS	GBE1_MDI3-	S27	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
10	GND	Power	GND	S25	Digital ground
11	3V3	Power	3V3	11	Internal 3V3 Power Supply
12	3V3	O OD CMOS	GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity
13	3V3	Power	3V3	13	Internal 3V3 Power Supply
14	3V3	O CMOS	GBE1_LINK100	S19	GB Ethernet Link speed indication LED for 100 Mbps. Active low.
15	GND	Power	GND	15	Digital ground
16	GND	Power	GND	16	Digital ground
JCTL					
11	3V3	O OD CMOS	GBE0_LINK1000#	P22	Link speed indication LED for 1000 Mbps. Active low.
13	3V3	O OD CMOS	GBE1_LINK1000#	S22	Link speed indication LED for 1000 Mbps. Active low.

Table 11 Ethernet 10/100/1000 Mbps pins

Next figures show both ethernet connectors on the schematic design and the connectors location on the Base:

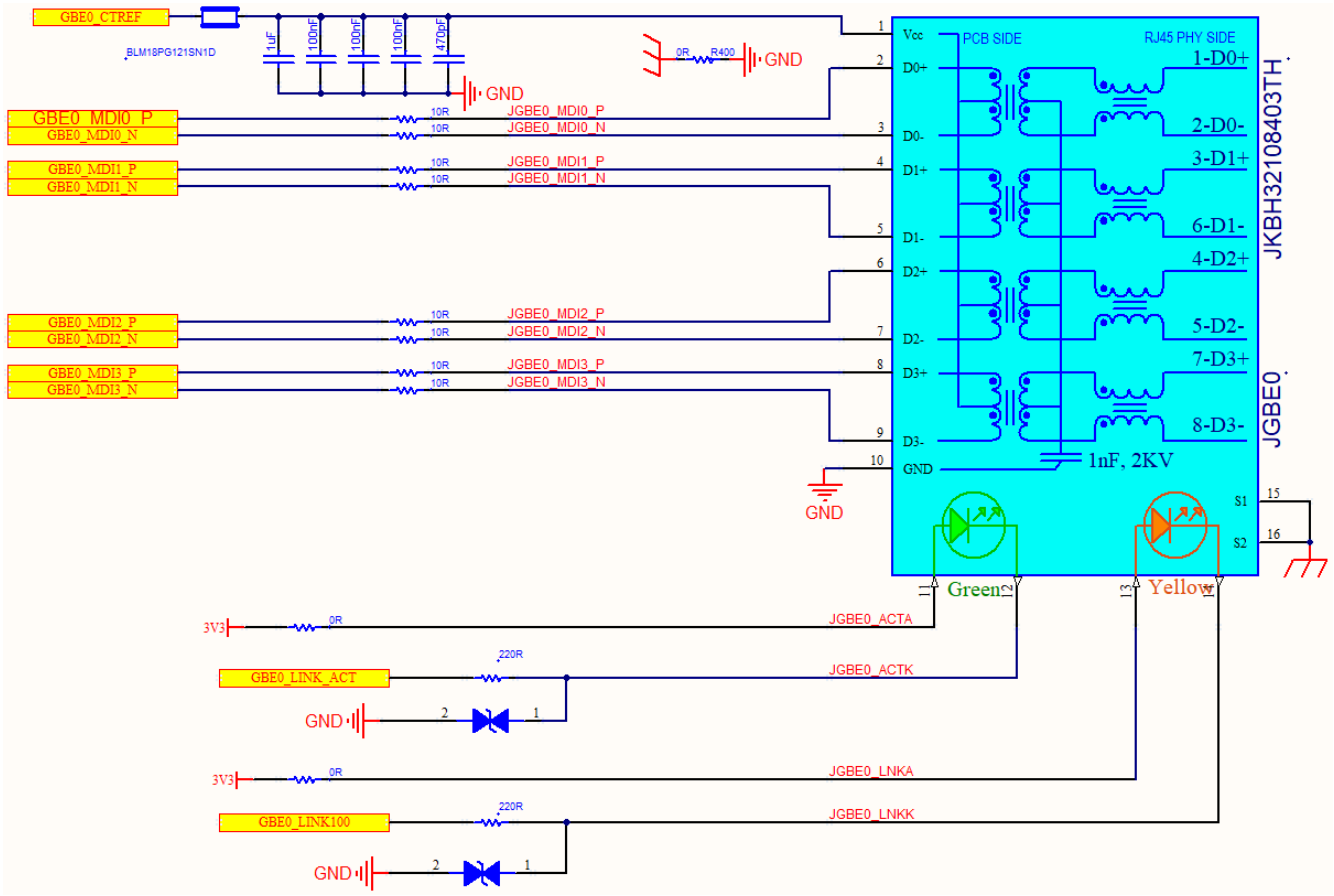


Figure 12 JGBE0 Ethernet connector schematic

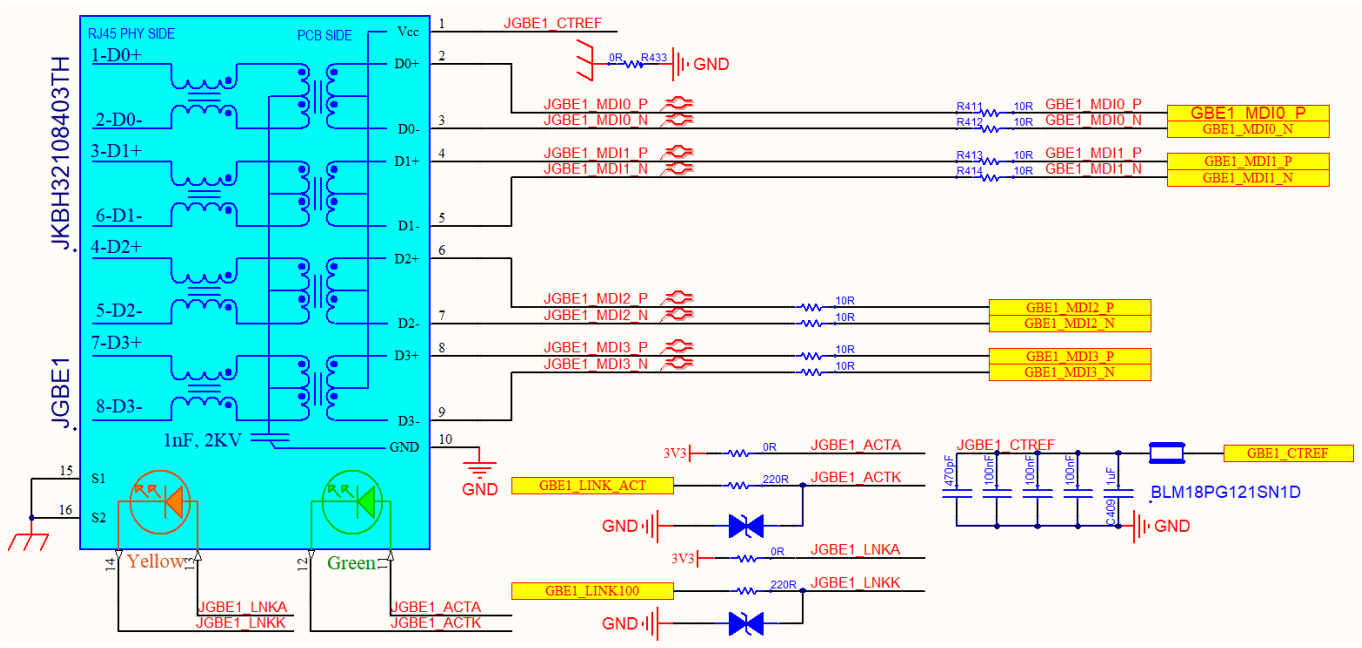


Figure 13 JGBE1 Ethernet connector schematic

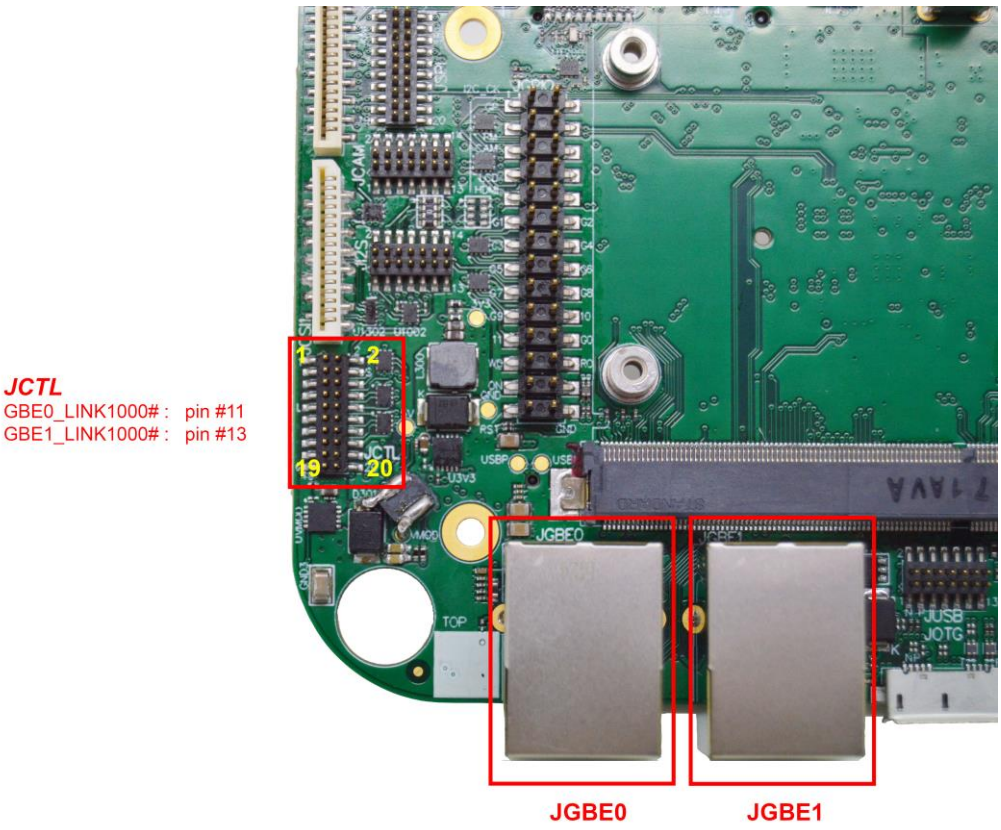
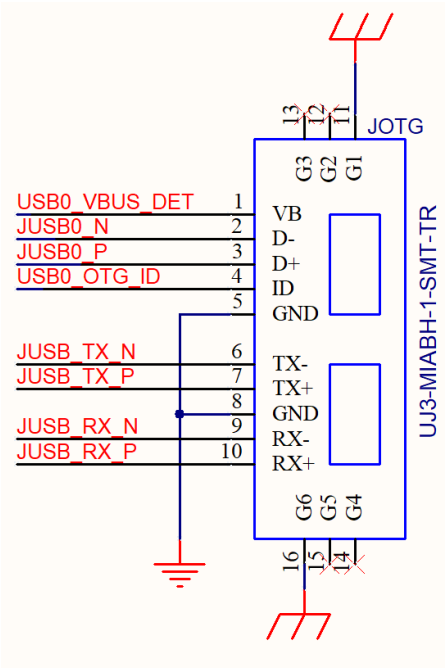


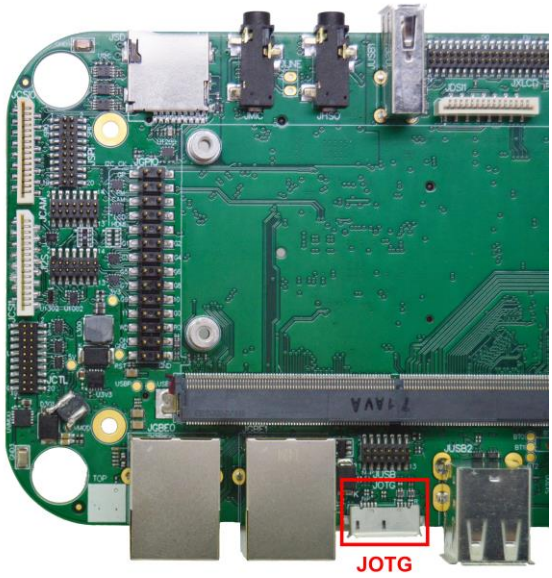
Figure 14 Ethernet Connectors (JGBE0 & JGBE1) Location

5.4 USB CONNECTIONS

5.4.1 USB 3.0 OTG

The Expansion Board includes a single USB 3.0 OTG port (connector JOTG), directly connected to the USB OTG pins of the IGEP™ SMARC family interface. This connector is an USB 3.0 type mini-AB receptacle connector, next figures shows the connection to this port and the location of the connector on the base:





The USB 3.0 OTG interface is implemented with the IGEP™ SMARC™ family USB OTG controller:

- Operates either as the function controller of a Super/High/Full Speed USB peripheral or as host in point-to-point or multipoint communications.
- Complies with the USB 3.0 standard for SuperSpeed (5 Gbps) function and with on-the-go (OTG) supplement.
- Supports USB 3.0 peripheral at SuperSpeed (5 Gbps), High Speed (480 Mbps) and Full Speed (12 Mbps).
- Supports USB 3.0 host at SuperSpeed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1,5 Mbps).

USB 3.0 OTG signals are available through next connector pins.

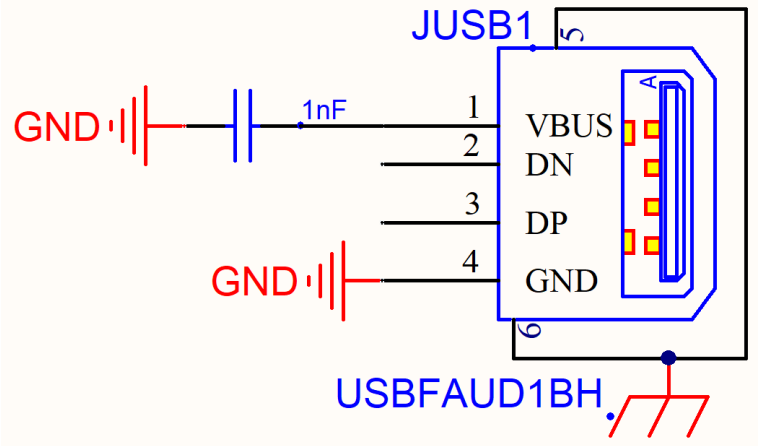
Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JOTG					
1	5V	Input	USB_OTG_VBUS	P63	USB-OTG: USB2.0 Host power detection when this port is used as a device.
2	USB	IO	USB0-	P61	UBS-OTG: USB2.0 differential data input.
3	USB	IO	USB0+	P60	UBS-OTG: USB2.0 differential data input.
4	1V8	Input	USB_OTG_ID	P64	USB-OTG: USB2.0 OTG ID input, active high.
5	GND	Power	GND	S64	Digital ground
6	USB SS	Output	USB3_SSTX-	S63	USB3 SS: TX differential pair.
7	USB SS	Output	USB3_SSTX+	S62	USB3 SS: TX differential pair.

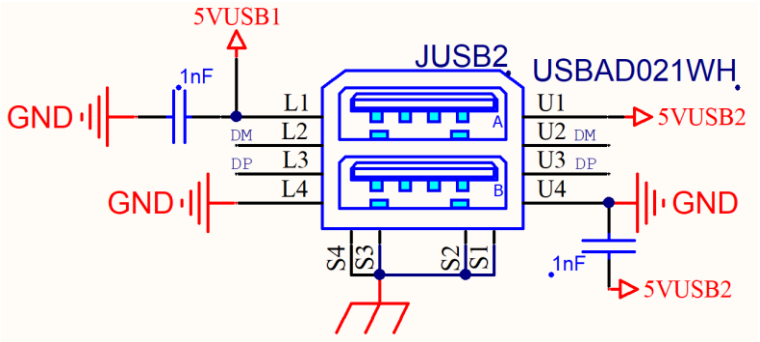
8	GND	Power	GND	S67	Digital ground
9	USB SS	Input	USB3_SSRX-	S66	USB1 SS: RX differential pair.
10	USB SS	Input	USB3_SSRX+	S65	USB1 SS: RX differential pair.
11	GND	Power	GND	S70	Digital ground
12	NC	NC	RESERVED		Not connected
13	NC	NC	RESERVED		Not connected
14	NC	NC	RESERVED		Not connected
15	NC	NC	RESERVED		Not connected
16	GND	Power	GND	S73	Digital ground

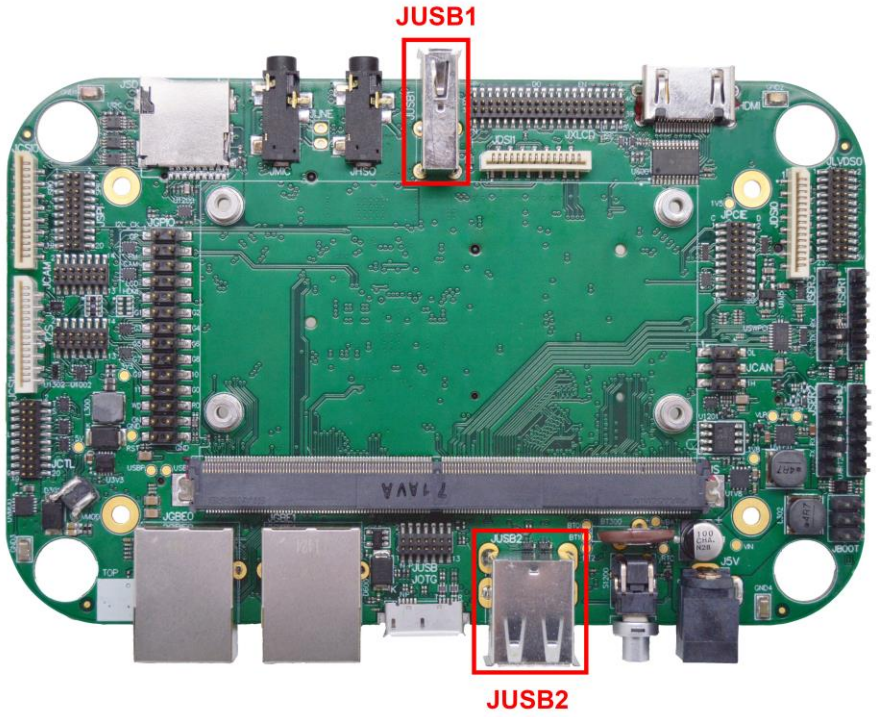
5.4.2 USB 2.0 Host

The BASE SMARC™ EXPANSION includes three USB 2.0 ports available through Type A connectors JUSB1 and JUSB2 (simple and double respectively). These are provided from the SMARC™ USB1 port and using a Hi-Speed Hub controller. Hardware provides power on/off switch control and up to 500 mA current limit at 5 V on each of the three ports.

Next figures show the connection to these ports.







The USB 2.0 Host signals are available through next connector pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JUSB1					
1	5V	Power	VDD_IN	P153	Pins used to power up the module. 4,75 V to 5,25 V
2	USB	IO	USB1-	P66	UBS1: USB2.0 differential data input. Internally used by HUB-3 (1)
3	USB	IO	USB1+	P65	UBS1: USB2.0 differential data input. Internally used by HUB-3 (1)
4	GND	Power	GND	P68	Digital ground
5	GND	Power	GND	P59	Digital ground
6	GND	Power	GND	P79	Digital ground
JUSB2					
L1	5V	Power	VDD_IN	P151	Pins used to power up the module. 4,75 V to 5,25 V
L2	USB	IO	USB1-	P66	UBS1: USB2.0 differential data input. Internally used by HUB-1 (1)
L3	USB	IO	USB1+	P65	UBS1: USB2.0 differential data input. Internally used by HUB-1 (1)
L4	GND	Power	GND	P68	Digital ground

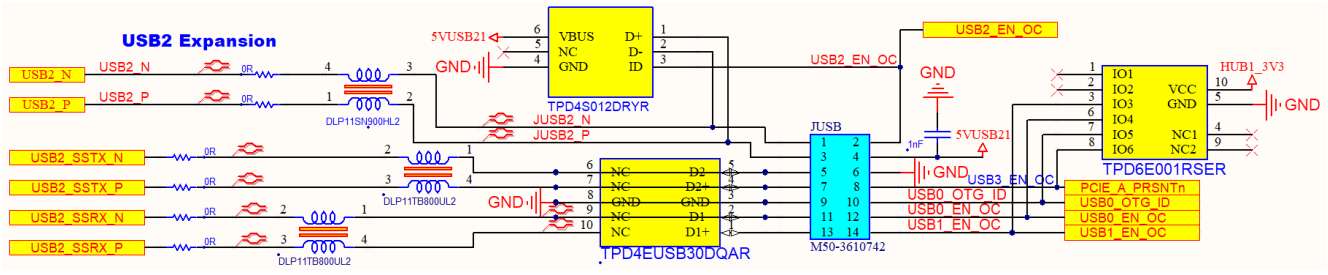
U1	5V	Power	VDD_IN	P152	Pins used to power up the module. 4,75 V to 5,25 V
U2	USB	IO	USB1-	P66	UBS1: USB2.0 differential data input. Internally used by HUB-2 (1)
U3	USB	IO	USB1+	P65	UBS1: USB2.0 differential data input. Internally used by HUB-2 (1)
U4	GND	Power	GND	P59	Digital ground
S1	GND	Power	GND	P79	Digital ground
S2	GND	Power	GND	P82	Digital ground
S3	GND	Power	GND	P85	Digital ground
S4	GND	Power	GND	P88	Digital ground
Notes					
(1)	USB HUB internal.				

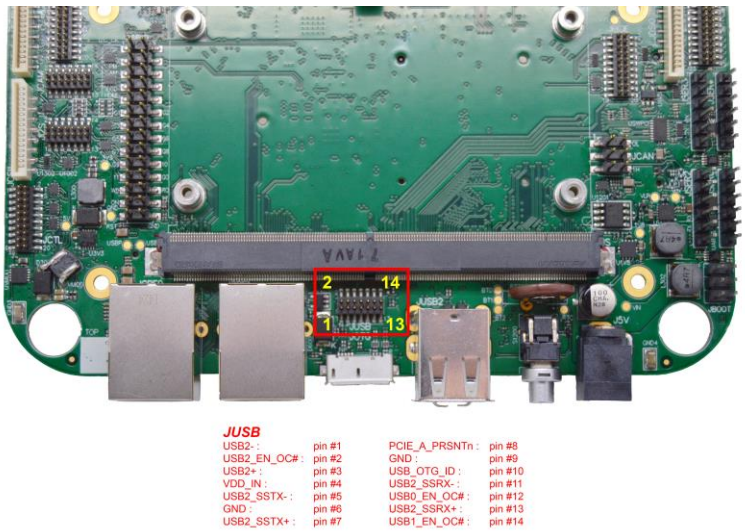
Table 12 USB 2.0 Host signals

5.4.3 USB Expansion Header

There is the possibility to use a last USB 3.0 OTG connection using the expansion header JUSB. With this, the developer can access to the SMARC™ USB2 port and implement his own USB port connector in case to need more ports.

Next figure shows an example about how to connect this added port.





USB Expansion signals are available on next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JUSB					
1	USB	IO	USB2-	P70	UBS2: USB2.0 differential data input.
2	3V3	IO OD	USB2_EN_OC#	P71	USB2: Enable OUT(active High)-Overcurrent IN(active Low) PIN (1)
3	USB	IO	USB2+	P69	UBS2: USB2.0 differential data input.
4	5V	Power	VDD_IN	P154	Pins used to power up the module. 4,75 V to 5,25 V
5	USB SS	Output	USB2_SSTX-	S72	USB2 SS: TX differential pair.
6	GND	Power	GND	S73	Digital ground
7	USB SS	Output	USB2_SSTX+	S71	USB2 SS: TX differential pair.
8	3V3	Input	PCIE_A_PRSNTn	P74	PCIE-A Present (active Low) (1)
9	GND	Power	GND	S70	Digital ground
10	1V8	Input	USB_OTG_ID	P64	USB-OTG: USB2.0 OTG ID input, active high.
11	USB SS	Input	USB2_SSRX-	S75	USB2 SS: RX differential pair.
12	3V3	IO OD	USB0_EN_OC#	P62	USB-OTG: Enable (active High)-Overcurrent (active Low) PIN (1)
13	USB SS	Input	USB2_SSRX+	S74	USB2 SS: RX differential pair.
14	3V3	IO OD	USB1_EN_OC#	P67	USB1: Enable OUT(active High)-Overcurrent IN(active Low) PIN (1)
Notes					
(1)	It is needed a 10k pull-up resistor.				

Table 13 USB Expansion signals

5.5 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

In the Expansion Board there are five I2C interfaces that can be found in header JGPIO. These can be used by the user but keeping in mind that are lines shared with functions defined in the SMARC™ documentation.

Next figure shows an example about how to use a I2C interface.

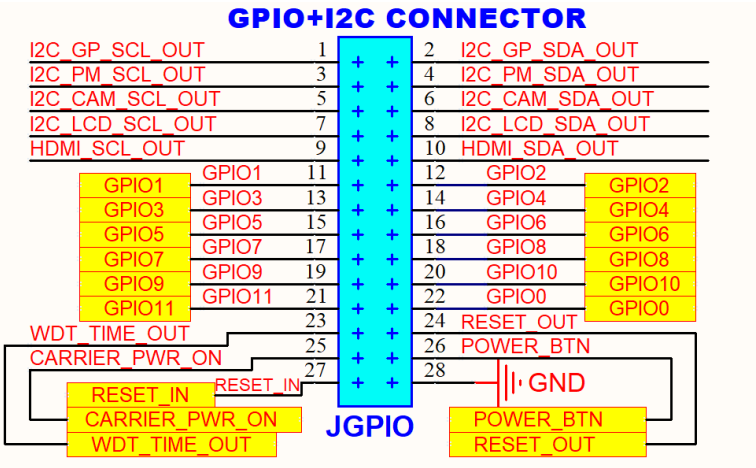


Figure 15 I2C connector schematics

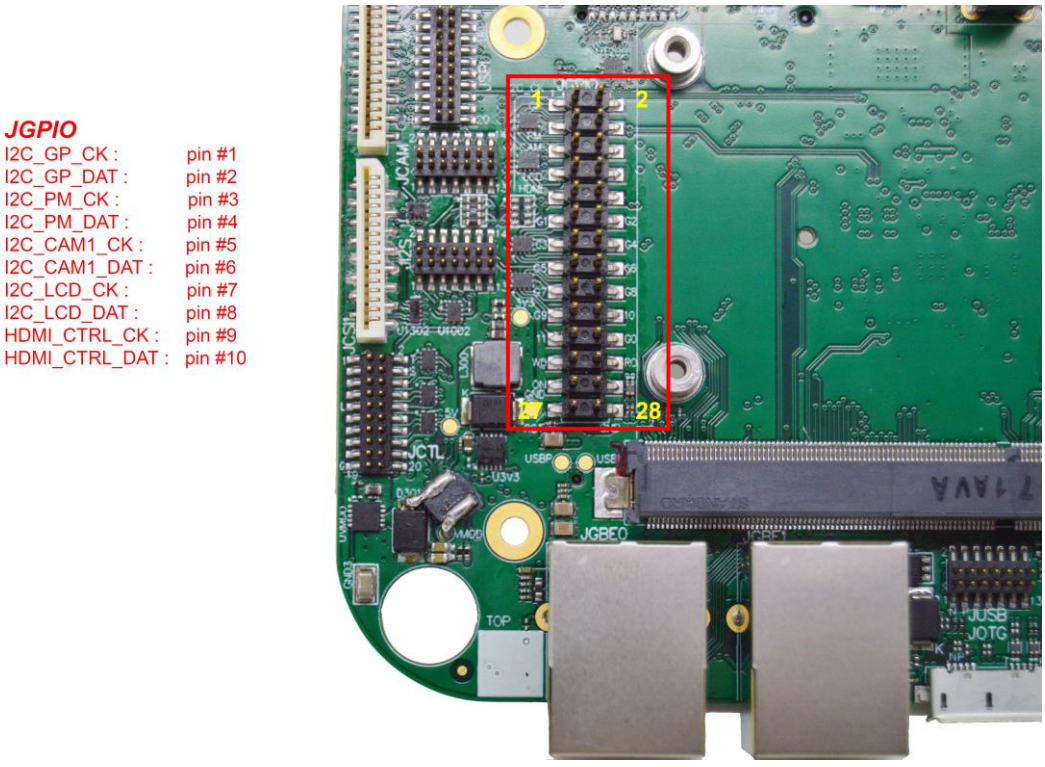


Figure 16 BASE SMARC™ EXPANSION: JGPIO – I2C pins

Next table shows the available signals related to I2C interfaces in connector JGPIO.

Conector Pin	Volt Level	Type	Function	JSMARC	Comments
JGPIO					
1	1V8	IO OD	I2C_GP_CK	S48	I2C General Purpose: Clock signal. Shared internally with CODEC
2	1V8	IO OD	I2C_GP_DAT	S49	I2C General Purpose: Data signal. Shared internally with CODEC
3	1V8	IO OD	I2C_PM_CK	P121	I2C2: Clock signal. Shared with internal EEPROM
4	1V8	IO OD	I2C_PM_DAT	P122	I2C2: Data signal. Shared with internal EEPROM
5	1V8	IO OD	I2C_CAM1_CK	S1,S5	I2C2: Clock signal. Shared with I2C_CAM_CK
6	1V8	IO OD	I2C_CAM1_DAT	S2,S7	I2C2: Data signal. Shared with I2C_CAM_DAT
7	1V8	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI
8	1V8	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI
9	1V8	Output OD	HDMI_CTRL_CK	P105	I2C Clock line dedicated to HDMI. Connected to I2C2_CLK
10	1V8	IO OD	HDMI_CTRL_DAT	P106	I2C Data line dedicated to HDMI. Connected to I2C2_SDA

Table 14 I2C signals

5.6 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the IGEP™ SMARC™ family modules to external peripherals. It is a full duplex synchronous bus, supporting a single master and up two devices each SPI peripheral.

In the header JSPI, there are present SPI0 and ESPI1 (this is an enhanced SPI bus). Next figure shows an example about how to connect this feature.

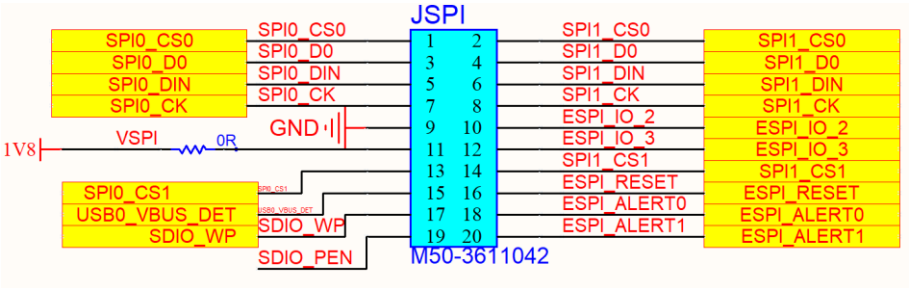


Figure 17 SPI connector schematics

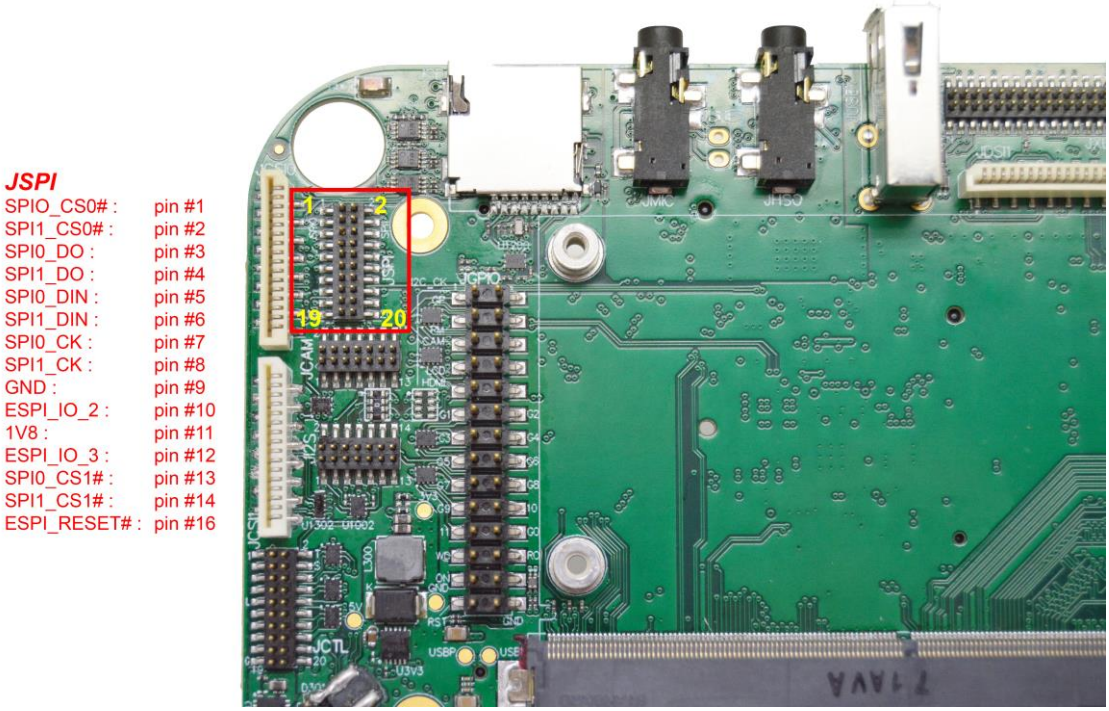


Figure 18 BASE SMARC™ EXPANSION: JSPI – SPI header

Next table shows the available signals related to SPI function in connector JSPI. Please, be careful that there are some pins not used for this feature but present in other chapters of this document.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JSPI					
1	1V8	Output	SPI0_CS0#	P43	SPI0 Interface: Master Chip Select 0. Active low.
2	1V8	Output	SPI1_CS0#	P54	SPI1 Interface: Master Chip Select 0. Active low.
3	1V8	Output	SPI0_DO	P46	SPI0 Interface: Master Data Output.
4	1V8	Output	SPI1_DO	P58	SPI1 Interface: Master Data Output.
5	1V8	Input	SPI0_DIN	P45	SPI0 Interface: Master Data Input.
6	1V8	Input	SPI1_DIN	P57	SPI1 Interface: Master Data Input.
7	1V8	Output	SPI0_CK	P44	SPI0 Interface: Clock.
8	1V8	Output	SPI1_CK	P56	SPI1 Interface: Clock.
9	GND	Power	GND	P38	Digital ground
10	1V8	IO	ESPI_IO_2	S56	ESPI Input-Output Data 2
11	1V8	Power	1V8	1V8	Internal 1V8 Power Supply
12	1V8	IO	ESPI_IO_3	S57	ESPI Input-Output Data 3

13	1V8	Output	SPI0_CS1#	P31	SPI0 Interface: Master Chip Select 1. Active low.
14	1V8	Output	SPI1_CS1#	P55	SPI1 Interface: Master Chip Select 1. Active low.
16	1V8	Output	ESPI_RESET#	S58	ESPI Reset; Active Low

Table 15 SPI signals

5.7 I2S: SERIAL AUDIO PORT

There are available two digital audio ports (I2S1 and I2S2) through the header JI2S. These can be used for interfacing digital audio devices as Audio CODECs and DSP chips.

Next figure shows and example to use a I2S port.

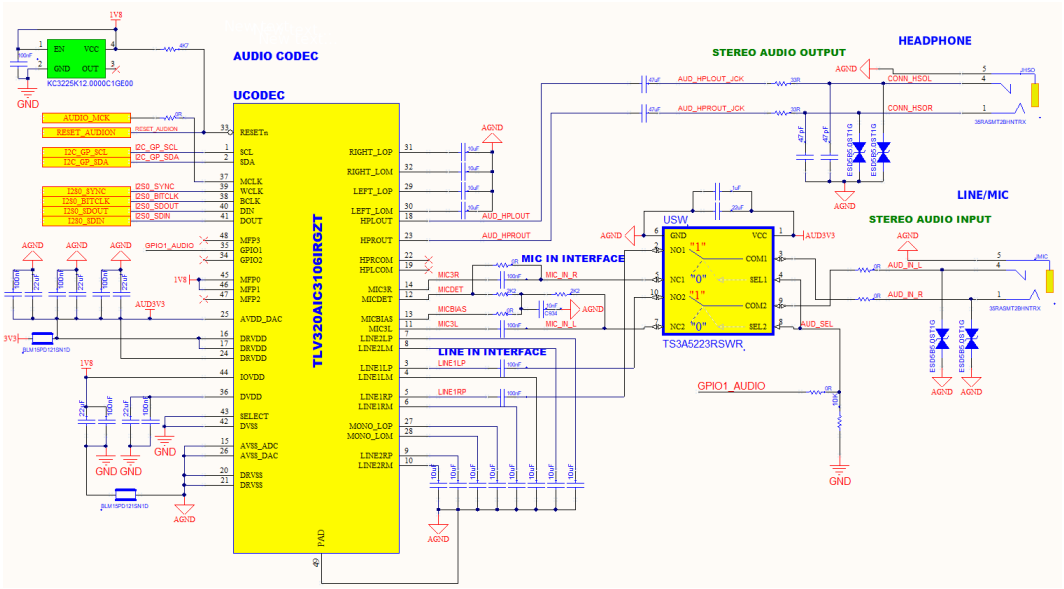


Figure 19 I2S port example: Audio codec schematics

The BASE SMARC™ EXPANSION uses port I2S0 from SMARC™ connector to offer, through an internal Audio CODEC, Stereo Audio output and input (respectively on connectors JHSO, Headphone, and JMIC, Line/Mic).

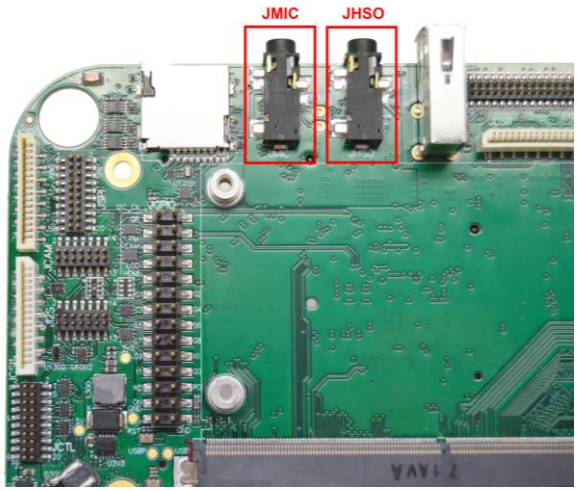


Figure 20 BASE SMARC™ EXPANSION: I2S / JMIC & JHSO – Audio Line In and Line Out connectors

There are also available two I2S ports (I2S1 and I2S2) to be configured by the User in the JI2S header.

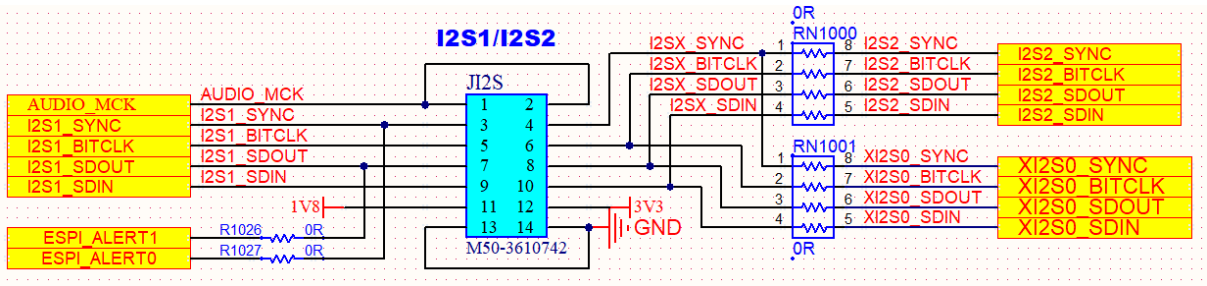


Figure 21 I2S port schematics

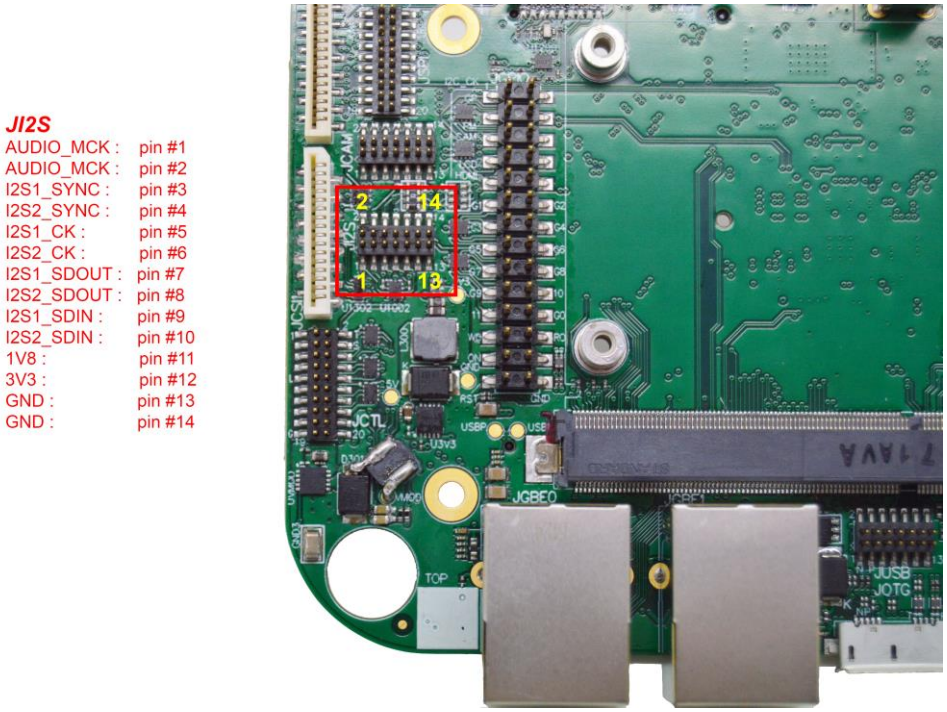


Figure 22 BASE SMARC™ EXPANSION: JI2S – I2S header

Next table shows the available signals related to I2S ports in connector JI2S.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JI2S					
1	1V8	Output	AUDIO_MCK	S38	Audio Digital Master Clock. Used internally by CODEC.
2	1V8	Output	AUDIO_MCK	S38	Audio Digital Master Clock. Used internally by CODEC.
3	1V8	IO	I2S1_SYNC	S43	I2S1 Left & Right Audio synchronization clock.
4	1V8	IO	I2S2_SYNC	S50	I2S2 Left & Right Audio synchronization clock.
5	1V8	IO	I2S1_CK	S46	I2S1 Digital Audio BIT clock.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
6	1V8	IO	I2S2_CK	S53	I2S2 Digital Audio BIT clock.
7	1V8	Output	I2S1_SDOUT	S44	I2S1 Digital Audio output.
8	1V8	Output	I2S2_SDOUT	S51	I2S2 Digital Audio output.
9	1V8	Input	I2S1_SDIN	S45	I2S1 Digital Audio input.
10	1V8	Input	I2S2_SDIN	S52	I2S2 Digital Audio input.
11	1V8	Power	1V8	1V8	Internal 1V8 Power Supply
12	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
13	GND	Power	GND	S47	Digital ground
14	GND	Power	GND	S61	Digital ground

Table 16 I2S signals

5.8 MICRO-SD CONNECTOR

The BASE SMARC™ EXPANSION includes a micro-SD connector (JSD2). Next figure shows connections.

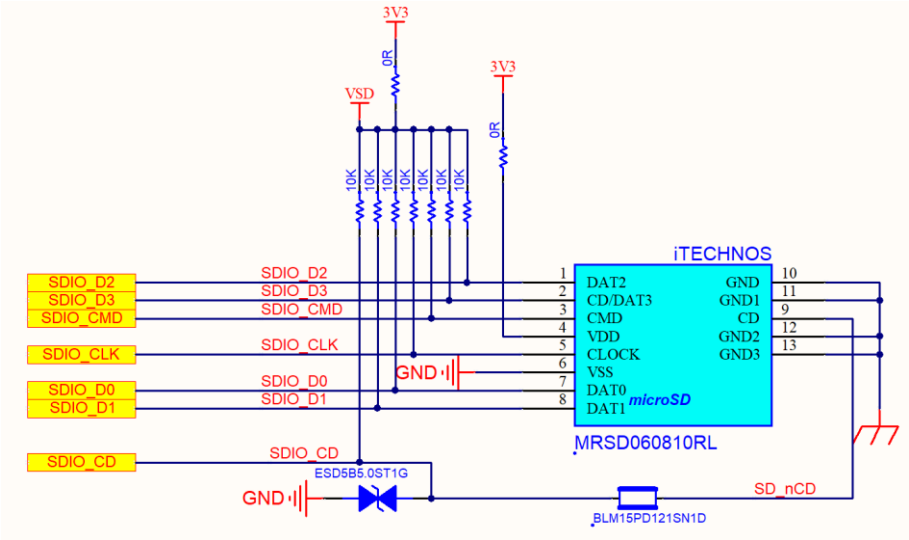


Figure 23 Micro-SD schematic

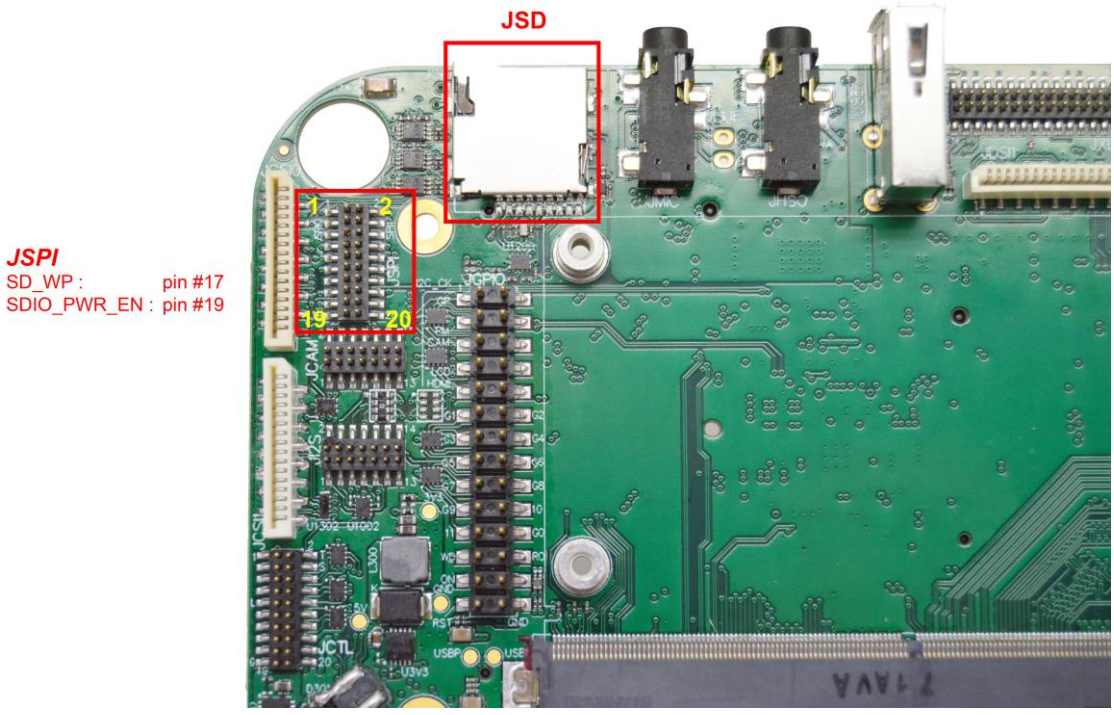


Figure 24 BASE SMARC™ EXPANSION: JSD – SD-card connector

Micro-SD connector signals are available through next connection pins. Please, be careful with some signals that has been to be placed in other free connector or headers.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JSD					
1	3V3	IO	SDIO_D2	P41	SD card 4-bit Interface: data path (D2).
2	3V3	IO	SDIO_D3	P42	SD card 4-bit Interface: data path (D3).
3	3V3	IO	SDIO_CMD	P34	SD card 4-bit Interface: Command Line.
4	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
5	3V3	Output	SDIO_CK	P36	SD card 4-bit Interface: Clock.
6	GND	Power	GND	P32	Digital ground
7	3V3	IO	SDIO_D0	P39	SD card 4-bit Interface: data path (D0).
8	3V3	IO	SDIO_D1	P40	SD card 4-bit Interface: data path (D1).
9	GND	Power	GND	P38	Digital ground
10	3V3	Input	SDIO_CD#	P35	SD card 4-bit Interface: Card Detect. This pin may vary with SD connector manufacturer
11	GND	Power	GND	P47	Digital ground
12	GND	Power	GND	P50	Digital ground
13	GND	Power	GND	P53	Digital ground
14	GND	Power	GND	P59	Digital ground
JSPI					
17	3V3	Input	SD_WP	P33	SD Card Write Protect (1)
19	3V3	Output	SDIO_PWR_EN	P37	SD Power Enable
Notes					
(1)	It is needed a 10k pull-up resistor.				

Table 17 Micro-SD connector signals (based on iTechnos MRSD060810RL)

5.9 SERIAL HEADER EXPANSION

The BASE SMARC™ EXPANSION includes serial expansion headers (JSER0, HSER1, JSER2 and JSER3) which are a single row 6-pin 2,54 mm male header.

These can be accessed using a sinple USB-serial adaptor. Please, be careful because these are directly connected to the UART of processor.

Next figure shows the four serial header expansion connections.

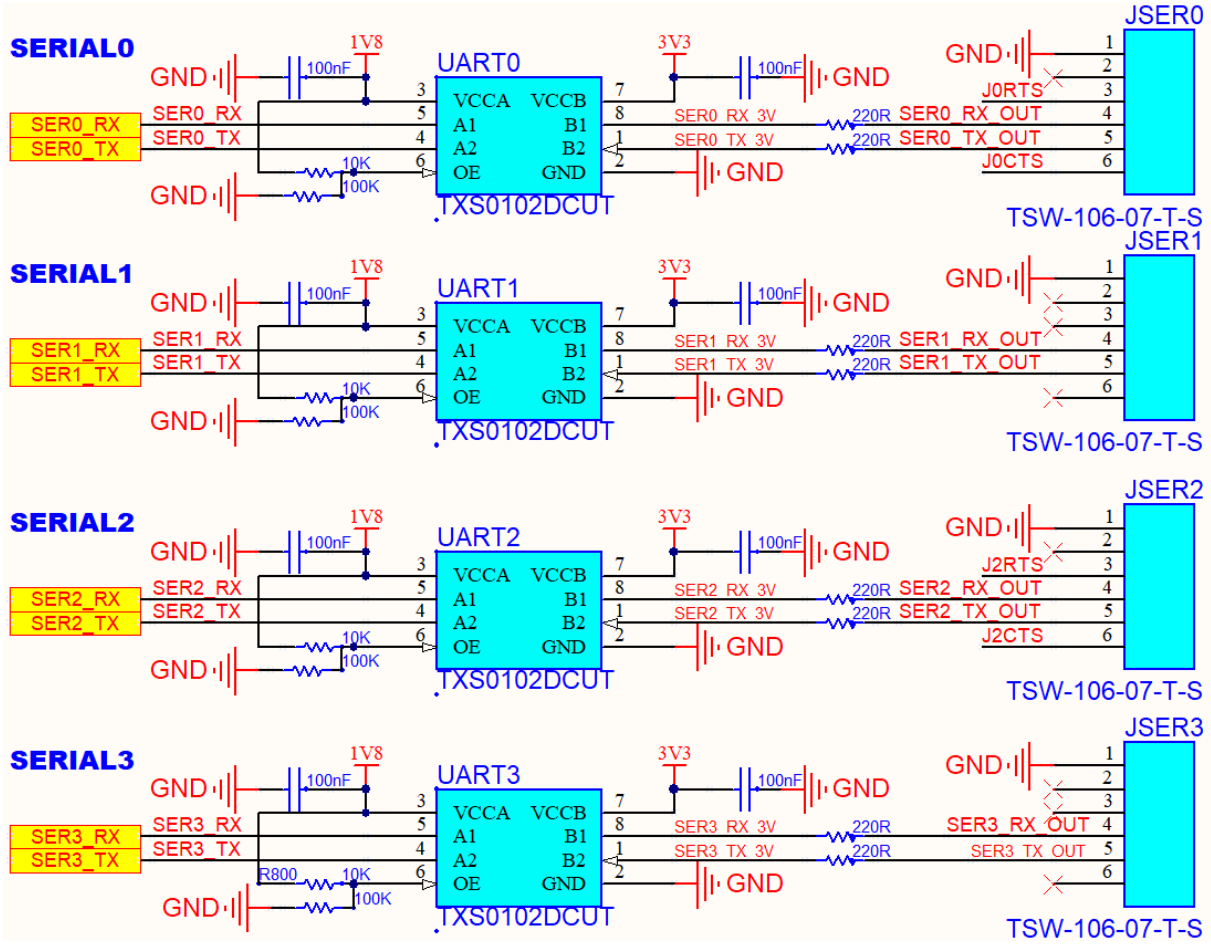


Figure 25 Serial header expansion schematics

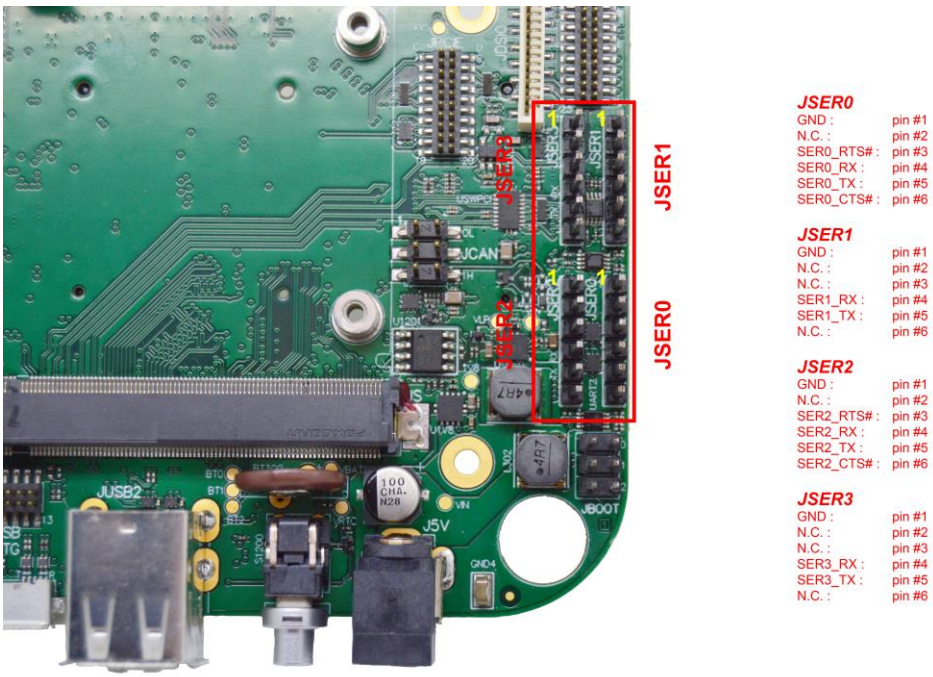


Figure 26 BASE SMARC™ EXPANSION: JSER0, JSER1, JSER2 & JSER3 – Serial expansion headers

Signals are available through next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JSER0					
1	GND	Power	GND	P133	Digital ground
2	NC	NC	Not Connected		Not used
3	3V3	Output	SER0_RTS#	P131	SERIAL-0: Request to Send handshake line. Active low. (1)
4	3V3	Input	SER0_RX	P130	SERIAL-0: Asynchronous serial port 4 data in. (1)
5	3V3	Output	SER0_TX	P129	SERIAL-0: Asynchronous serial port 4 data out. (1)
6	3V3	Input	SER0_CTS#	P132	SERIAL-0: Clear to Send handshake line. Active low. (1)
JSER1					
1	GND	Power	GND	P133	Digital ground
2	NC	NC	Not Connected		Not used
3	NC	NC	Not Connected		Not used
4	3V3	Input	SER1_RX	P135	SERIAL-1: Asynchronous serial port 4 data in. (1)
5	3V3	Output	SER1_TX	P134	SERIAL-1: Asynchronous serial port 4 data out. (1)

6	NC	NC	Not Connected		Not used
JSER2					
1	GND	Power	GND	P133	Digital ground
2	NC	NC	Not Connected		Not used
3	3V3	Output	SER2_RTS#	P138	SERIAL-2: Request to Send handshake line. Active low. (1)
4	3V3	Input	SER2_RX	P137	SERIAL-2: Asynchronous serial port 4 data in. (1)
5	3V3	Output	SER2_TX	P136	SERIAL-2: Asynchronous serial port 4 data out. (1)
6	3V3	Input	SER2_CTS#	P139	SERIAL-2: Clear to Send handshake line. Active low. (1)
JSER3					
1	GND	Power	GND	P133	Digital ground
2	NC	NC	Not Connected		Not used
3	NC	NC	NOT CONNECTED		Not used
4	3V3	Input	SER3_RX	P141	SERIAL-3: Asynchronous serial port 4 data in. (1)
5	3V3	Output	SER3_TX	P140	SERIAL-3: Asynchronous serial port 4 data out. (1)
6	NC	NC	Not Connected		Not used
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 18 Serial expansion signals

5.10 LCD AND TOUCHSCREEN CONNECTORS

The expansion board is prepared to connect a 24-bit LCD screen with touchscreen. This is a 5” model (RK050BR62-CT, by Rocktech Displays Ltd). Connection can be done though connectors JLCD and JTOUCH. Next figure shows how are defined connection of signals.

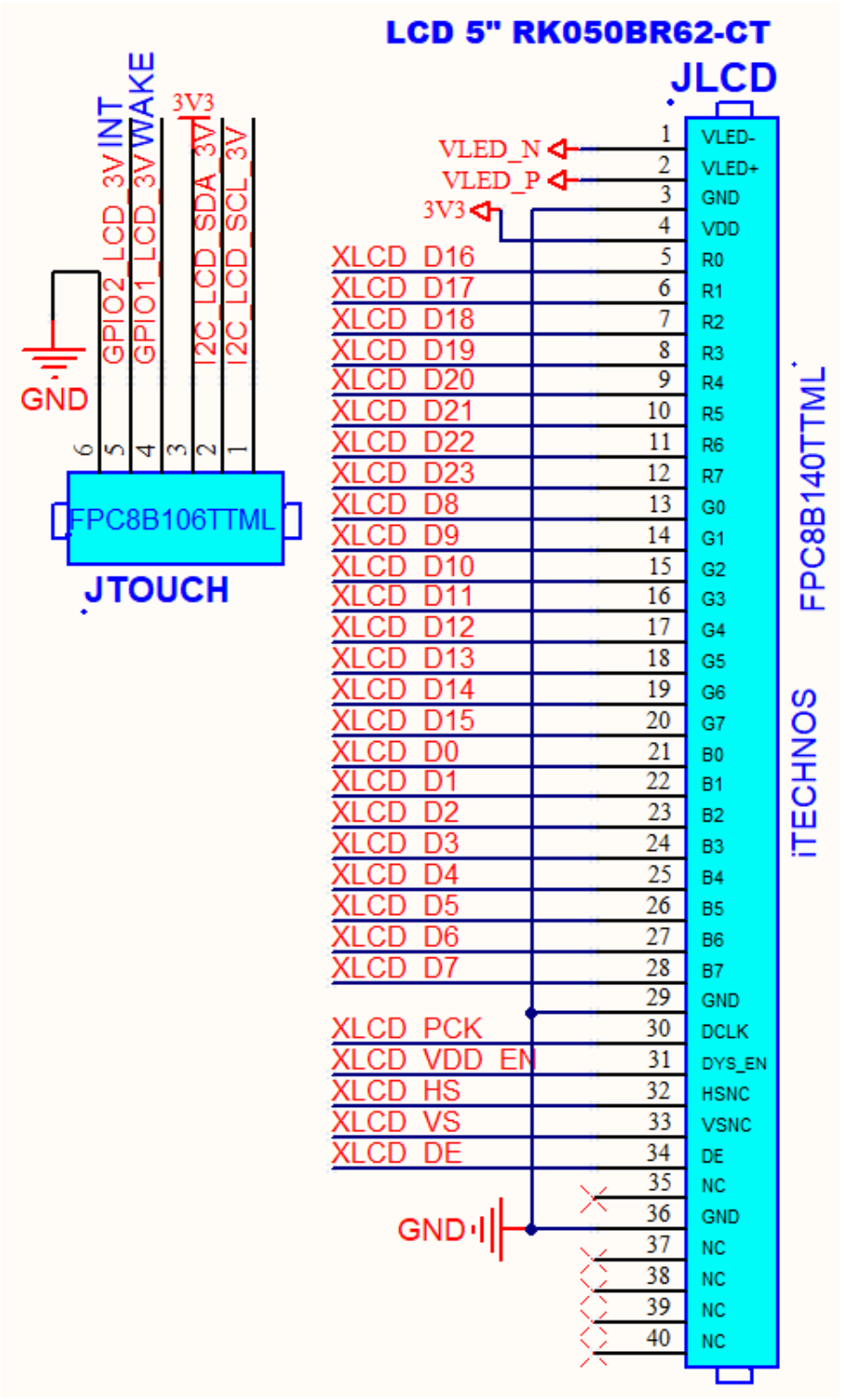


Figure 27 LCD and Touchscreen schematics

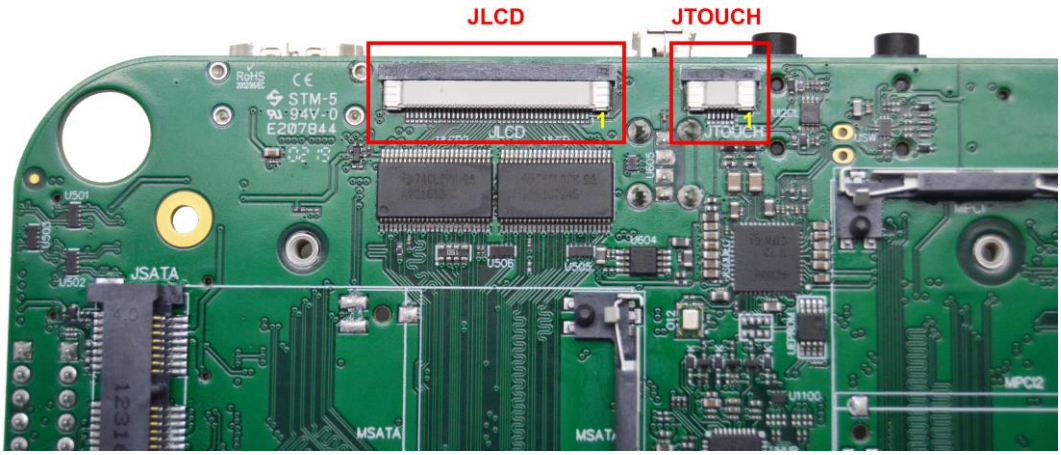


Figure 28 BASE SMARC™ EXPANSION: LCD & Touchscreen – JLCD & JTOUCH connectors

All these signals are available through next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JLCD					
1	1,23V	Power	1,23V	VLED_N	Internal 1,23V Power Supply
2	19V	Power	19V	VLED_P	Internal 19V Power Supply
3	GND	Power	GND	S101	Digital ground
4	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
5	3V3	Output	LCD_D16	S111	DiSPLAY DATA BIT (1)
6	3V3	Output	LCD_D17	S112	DiSPLAY DATA BIT (1)
7	3V3	Output	LCD_D18	S113	DiSPLAY DATA BIT (1)
8	3V3	Output	LCD_D19	S114	DiSPLAY DATA BIT (1)
9	3V3	Output	LCD_D20	S115	DiSPLAY DATA BIT (1)
10	3V3	Output	LCD_D21	S116	DiSPLAY DATA BIT (1)
11	3V3	Output	LCD_D22	S117	DiSPLAY DATA BIT (1)
12	3V3	Output	LCD_D23	S118	DiSPLAY DATA BIT (1)
13	3V3	Output	LCD_D8	S102	DiSPLAY DATA BIT (1)
14	3V3	Output	LCD_D9	S103	DiSPLAY DATA BIT (1)
15	3V3	Output	LCD_D10	S104	DiSPLAY DATA BIT (1)
16	3V3	Output	LCD_D11	S105	DiSPLAY DATA BIT (1)
17	3V3	Output	LCD_D12	S106	DiSPLAY DATA BIT (1)
18	3V3	Output	LCD_D13	S107	DiSPLAY DATA BIT (1)

19	3V3	Output	LCD_D14	S108	DiSPLAY DATA BIT (1)
20	3V3	Output	LCD_D15	S109	DiSPLAY DATA BIT (1)
21	3V3	Output	LCD_D0	S93	DiSPLAY DATA BIT (1)
22	3V3	Output	LCD_D1	S94	DiSPLAY DATA BIT (1)
23	3V3	Output	LCD_D2	S95	DiSPLAY DATA BIT (1)
24	3V3	Output	LCD_D3	S96	DiSPLAY DATA BIT (1)
25	3V3	Output	LCD_D4	S97	DiSPLAY DATA BIT (1)
26	3V3	Output	LCD_D5	S98	DiSPLAY DATA BIT (1)
27	3V3	Output	LCD_D6	S99	DiSPLAY DATA BIT (1)
28	3V3	Output	LCD_D7	S100	DiSPLAY DATA BIT (1)
29	GND	Power	GND	S110	Digital ground
30	3V3	Output	LCD_PCK	S123	DISPLAY PIXEL CLOCK (1)
31	3V3	Output	LCD_VDD_EN	S133	GPIO4[20] LCD Panel Power Enable. Internally used by LCD regulator (Active Low) (1)
32	3V3	Output	LCD_HS	S122	DISPLAY HORIZONTAL SYNCHRONISM (1)
33	3V3	Output	LCD_VS	S121	DISPLAY VERTICAL SYNCHRONISM (1)
34	3V3	Output	LCD_DE	S120	DISPLAY DATA READY (1)
35	NC	NC	Not Connected		Not used
36	GND	Power	GND	S119	Digital ground
37	NC	NC	Not Connected		Not used
38	NC	NC	Not Connected		Not used
39	NC	NC	Not Connected		Not used
40	NC	NC	Not Connected		Not used
JTOUCH					
1	3V3	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI (1)
2	3V3	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI (1)
3	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
4	3V3	IO	GPIO0	P108	General Purpose Input Output / CAM0 Power (1)

5	3V3	IO	GPIO2	P110	General Purpose Input Output / CAM0 Reset (Internal Enable-2 USB; Active High) (1)
6	GND	Power	GND		Digital ground
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 19 LCD & Touchscreen signals

In case that the Users wish to use a different model, there are also available the LCD signals through connector JXLCD. With this, Developers can test directly the chosen model in their final applications.

All these signals are available through next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JXLCD					
1	1,23V	Power	1,23V	VLED_N	Internal 1,23V Power Supply
2	19V	Power	19V	VLED_P	Internal 19V Power Supply
3	3V3	Output	LCD_BKLT_EN	S127	LCD Panel Backlite Enable (1)
4	3V3	Output	LCD_D8	S102	DiSPLAY DATA BIT (1)
5	3V3	Output	LCD_D18	S113	DiSPLAY DATA BIT (1)
6	3V3	Output	LCD_D9	S103	DiSPLAY DATA BIT (1)
7	3V3	Output	LCD_D16	S111	DiSPLAY DATA BIT (1)
8	3V3	Output	LCD_D17	S112	DiSPLAY DATA BIT (1)
9	3V3	Output	LCD_D21	S116	DiSPLAY DATA BIT (1)
10	3V3	Output	LCD_D10	S104	DiSPLAY DATA BIT (1)
11	3V3	Output	LCD_D20	S115	DiSPLAY DATA BIT (1)
12	3V3	Output	LCD_D19	S114	DiSPLAY DATA BIT (1)
13	3V3	Output	LCD_D22	S117	DiSPLAY DATA BIT (1)
14	3V3	Output	LCD_D23	S118	DiSPLAY DATA BIT (1)
15	3V3	Output	LCD_D11	S105	DiSPLAY DATA BIT (1)
16	3V3	Output	LCD_D12	S106	DiSPLAY DATA BIT (1)
17	3V3	Output	LCD_D13	S107	DiSPLAY DATA BIT (1)
18	3V3	Output	LCD_D0	S93	DiSPLAY DATA BIT (1)
19	3V3	Output	LCD_D15	S109	DiSPLAY DATA BIT (1)
20	3V3	Output	LCD_D14	S108	DiSPLAY DATA BIT (1)

21	3V3	Output	LCD_D1	S94	DiSPLAY DATA BIT (1)
22	3V3	Output	LCD_D2	S95	DiSPLAY DATA BIT (1)
23	3V3	Output	LCD_D3	S96	DiSPLAY DATA BIT (1)
24	3V3	Output	LCD_D4	S97	DiSPLAY DATA BIT (1)
25	3V3	Output	LCD_D5	S98	DiSPLAY DATA BIT (1)
26	3V3	Output	LCD_D6	S99	DiSPLAY DATA BIT (1)
27	3V3	Output	LCD_PCK	S123	DISPLAY PIXEL CLOCK (1)
28	3V3	Output	LCD_D7	S100	DiSPLAY DATA BIT (1)
29	3V3	Output	LCD_HS	S122	DISPLAY HORIZONTAL SYNCHRONISM (1)
30	3V3	Output	LCD_VDD_EN	S133	GPIO4[20] LCD Panel Power Enable. Internally used by LCD regulator (Active Low) (1)
31	3V3	Output	LCD_DE	S120	DISPLAY DATA READY (1)
32	3V3	Output	LCD_VS	S121	DISPLAY VERTICAL SYNCHRONISM (1)
33	3V3	IO	LCD_BKLT_PWM	S141	PWM signal for LCD Panel Backlite. Internally used by LCD regulator (1)
34	3V3	IO	GPIO0	P108	General Purpose Input Output / CAM0 Power (1)
35	3V3	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI (1)
36	3V3	IO	GPIO2	P110	General Purpose Input Output / CAM0 Reset (Internal Enable-2 USB; Active High) (1)
37	3V3	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI (1)
38	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
39	5V	Power	5V	P148	Internal 5V Power Supply
40	GND	Power	GND	S101	Digital ground
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 20 JXLCD expansion connector signals

5.11 LVDS: LOW-VOLTAGE DIFFERENTIAL SIGNALING INTERFACE

In this expansion board is also possible transmit a signal to a display using a LVDS interface. This is available through JLVDS connector. Connector includes power supply (+5 V and +3V3, GND) and control signals in order to easily build and connect an adaptor board to your specific LVDS display. Next figure shows its schematics.

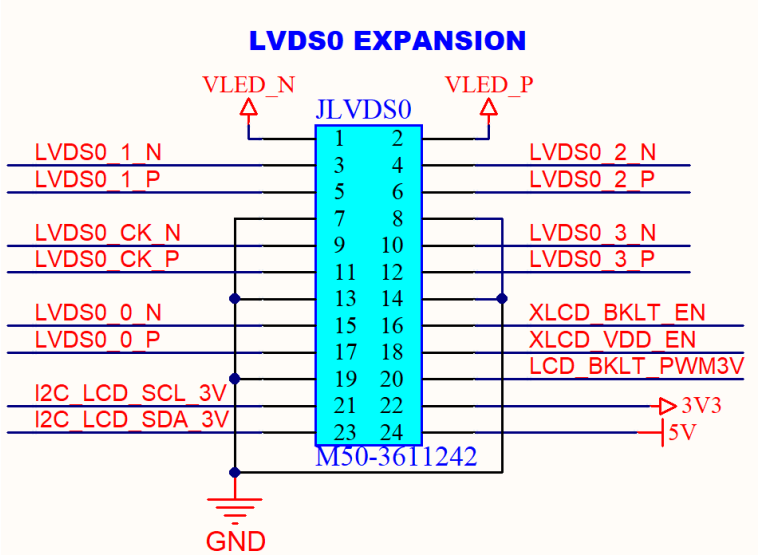


Figure 29 LVDS schematics

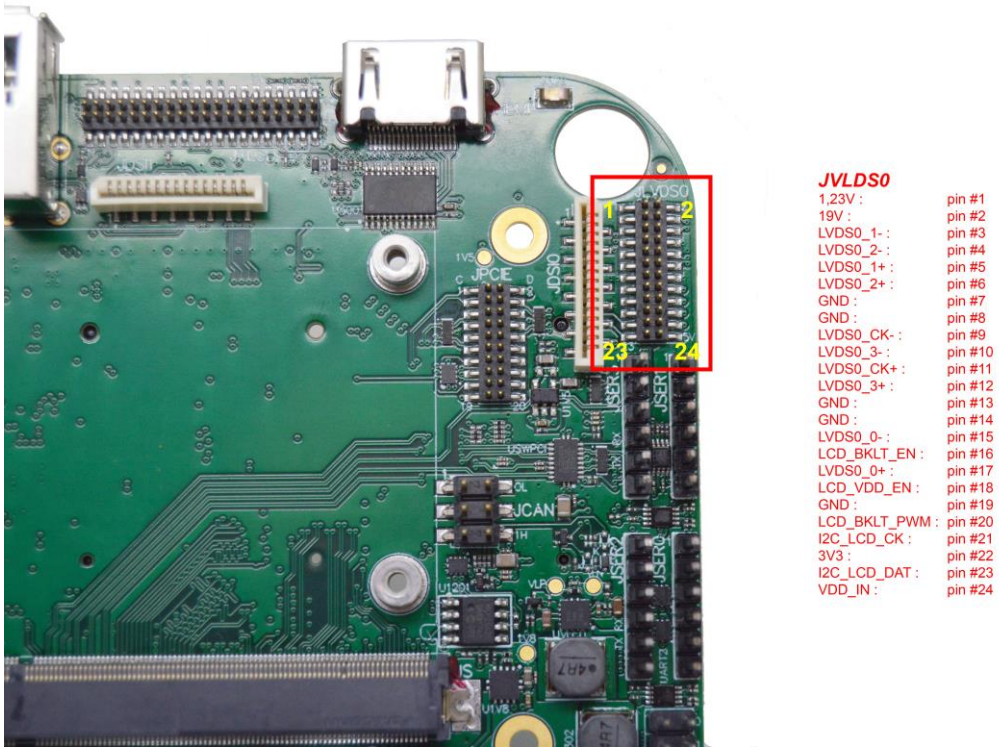


Figure 30 BASE SMARC™ EXPANSION: JLVDS0 – LVDS header

Signals are available through next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JLVDS					
1	1,23V	Power	1,23V	VLED_N	Internal 1,23V Power Supply
2	19V	Power	19V	VLED_P	Internal 19V Power Supply
3	LVDS D-PHY	Output	LVDS0_1-	S129	LVDS0: Data pair 1
4	LVDS D-PHY	Output	LVDS0_2-	S132	LVDS0: Data pair 2
5	LVDS D-PHY	Output	LVDS0_1+	S128	LVDS0: Data pair 1
6	LVDS D-PHY	Output	LVDS0_2+	S131	LVDS0: Data pair 2
7	GND	Power	GND	S130	Digital ground
8	GND	Power	GND	S136	Digital ground
9	LVDS D-PHY	Output	LVDS0_CK-	S135	LVDS0: Clock pair
10	LVDS D-PHY	Output	LVDS0_3-	S138	LVDS0: Data pair 3
11	LVDS D-PHY	Output	LVDS0_CK+	S134	LVDS0: Clock pair
12	LVDS D-PHY	Output	LVDS0_3+	S137	LVDS0: Data pair 3
13	GND	Power	GND		Digital ground
14	GND	Power	GND		Digital ground
15	LVDS D-PHY	Output	LVDS0_0-	S126	LVDS0: Data pair 0
16	3V3	Output	LCD_BKLT_EN	S127	LCD Panel Backlite Enable (1)
17	LVDS D-PHY	Output	LVDS0_0+	S125	LVDS0: Data pair 0
18	3V3	Output	LCD_VDD_EN	S133	GPIO4[20] LCD Panel Power Enable. Internally used by LCD regulator (Active Low) (1)
19	GND	Power	GND	S143	Digital ground
20	3V3	IO	LCD_BKLT_PWM	S141	PWM signal for LCD Panel Backlite. Internally used by LCD regulator (1)
21	3V3	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI (1)
22	3V3	Power	3V3	3V3	Internal 3V3 Power Supply

23	3V3	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI (1)
24	5V	Power	VDD_IN	P149	Pins used to power up the module. 4,75 V to 5,25 V
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 21 LVDS signals

5.12 DSI: DISPLAY SERIAL INTERFACE

There are available two serial display connectors (JDSI0 and JDSI1). Both of them are 2-lanes connectors. Next figure shows their schematics.

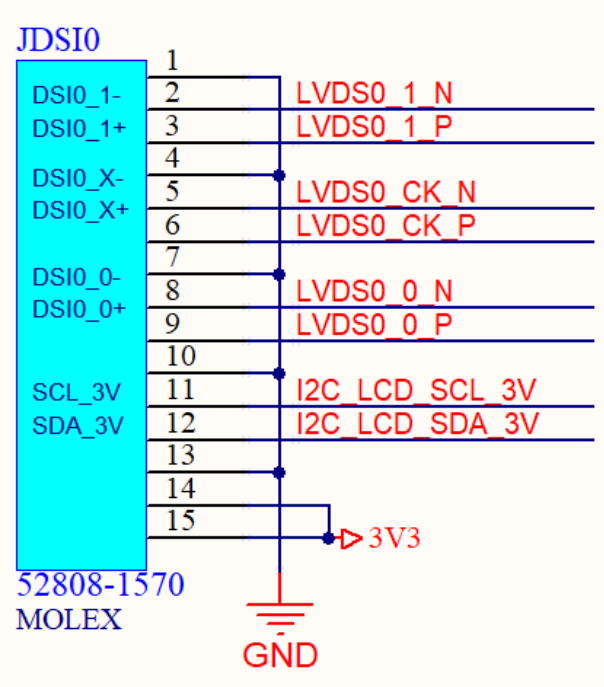


Figure 31 DSI0 connector schematics

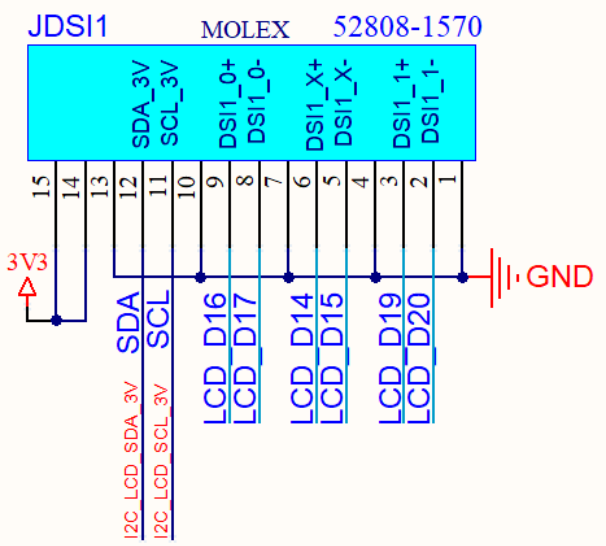


Figure 32 DSI1 connector schematics

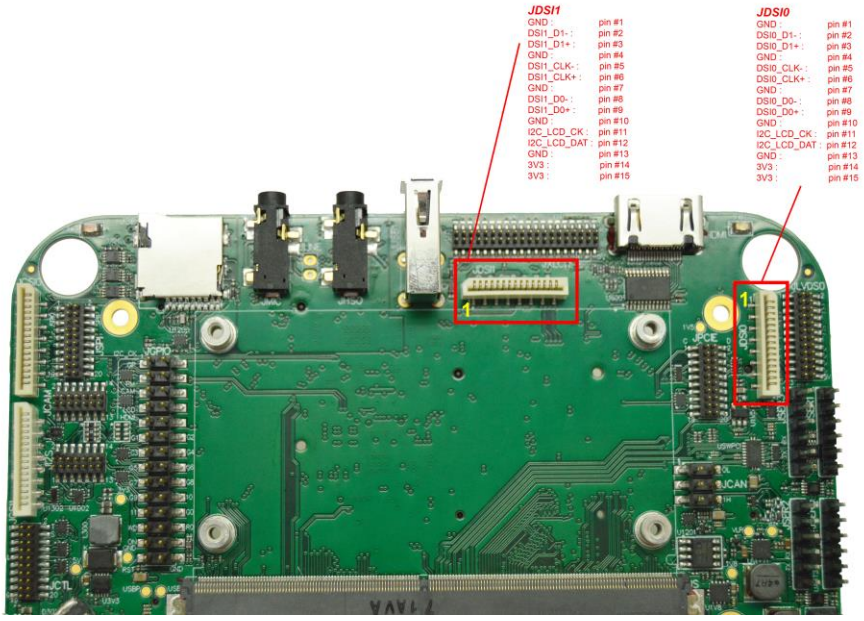


Figure 33 BASE SMARC™ EXPANSION: DSI – JDSI0, JDSI1 and JCTL connections

Their signals are available through next pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JDSI0					
1	GND	Power	GND	S130	Digital ground
2	LVDS D-PHY	Output	DSI0_D1-	S129	DSI: Data pair 1.
3	LVDS D-PHY	Output	DSI0_D1+	S128	DSI: Data pair 1.
4	GND	Power	GND	S110	Digital ground
5	LVDS D-PHY	Output	DSI0_CLK-	S135	DSI: Clock pair.

6	LVDS D-PHY	Output	DSI0_CLK+	S134	DSI: Clock pair.
7	GND	Power	GND	S119	Digital ground
8	LVDS D-PHY	Output	DSI0_D0-	S126	DSI: Data pair 0.
9	LVDS D-PHY	Output	DSI0_D0+	S125	DSI: Data pair 0.
10	GND	Power	GND	S124	Digital ground
11	3V3	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI (1)
12	3V3	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI (1)
13	GND	Power	GND	S130	Digital ground
14	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
15	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
JDSI1					
1	GND	Power	GND	S101	Digital ground
2	LVDS D-PHY	Output	DSI1_D1-	S115	DSI: Data pair 1.
3	LVDS D-PHY	Output	DSI1_D1+	S114	DSI: Data pair 1.
4	GND	Power	GND	S110	Digital ground
5	LVDS D-PHY	Output	DSI1_CLK-	S109	DSI: Clock pair.
6	LVDS D-PHY	Output	DSI1_CLK+	S108	DSI: Clock pair.
7	GND	Power	GND	S119	Digital ground
8	LVDS D-PHY	Output	DSI1_D0-	S112	DSI: Data pair 0.
9	LVDS D-PHY	Output	DSI1_D0+	S111	DSI: Data pair 0.
10	GND	Power	GND	S124	Digital ground
11	3V3	IO OD	I2C_LCD_CK	S139	I2C2: Clock signal. Shared with I2C_PM_CK, HDMI (1)
12	3V3	IO OD	I2C_LCD_DAT	S140	I2C2: Data signal. Shared with I2C_PM_DAT, HDMI (1)
13	GND	Power	GND	S130	Digital ground
14	3V3	Power	3V3	3V3	Internal 3V3 Power Supply
15	3V3	Power	3V3	3V3	Internal 3V3 Power Supply

Notes	
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.

Table 22 DSI0 and DSI1 signals

5.13 HDMI CONNECTOR

One of the video output possibilities in the BASE SMARC™ EXPANSION is through a HDMI type A receptacle connector (JHDMI). Next figure shows its connection.

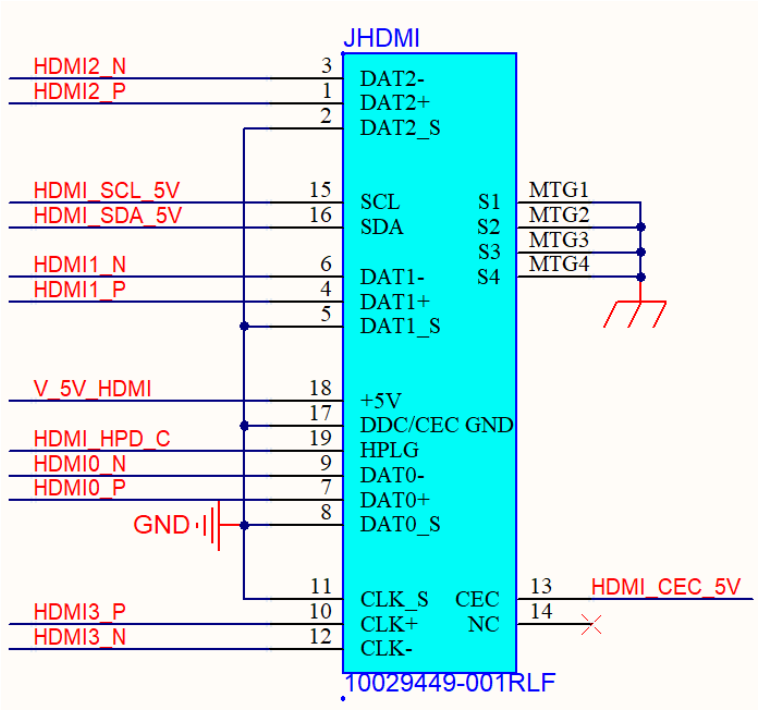


Figure 34 HDMI connector schematic

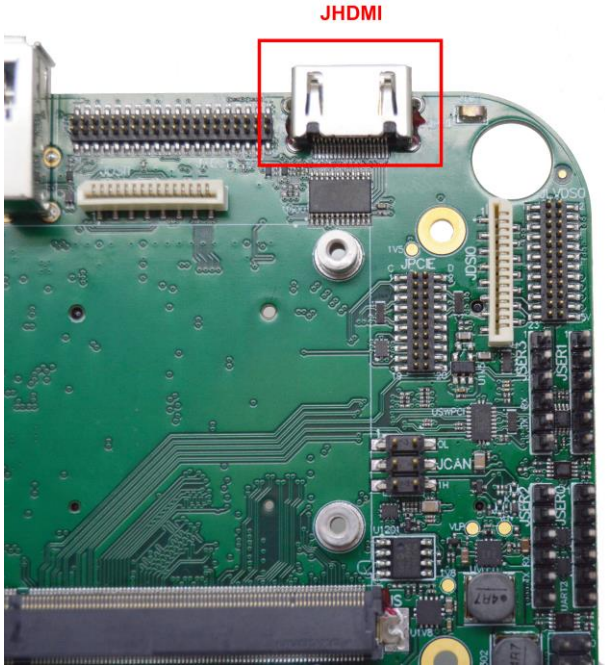


Figure 35 BASE SMARC™ EXPANSION: JHDMI – HDMI connector

HDMI signals are available through next connector pins.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JHDMI					
1	TMDS	Output	HDMI_D2+	P92	HDMI differential data input D2.
2	GND	Power	GND	P94	Digital ground
3	TMDS	Output	HDMI_D2-	P93	HDMI differential data input D2.
4	TMDS	Output	HDMI_D1+	P95	HDMI differential data input D1.
5	GND	Power	GND	P97	Digital ground
6	TMDS	Output	HDMI_D1-	P96	HDMI differential data input D1.
7	TMDS	Output	HDMI_D0+	P98	HDMI differential data input D0.
8	GND	Power	GND	P100	Digital ground
9	TMDS	Output	HDMI_D0-	P99	HDMI differential data input D0.
10	TMDS	Output	HDMI_CK+	P101	HDMI differential clock output pair.
11	GND	Power	GND	P103	Digital ground
12	TMDS	Output	HDMI_CK-	P102	HDMI differential clock output pair.
13	5V	IO	HDMI_CEC	P107	HDMI Consumer Electronic Control (1)
14	NC	NC	Not Connected		Not connected
15	5V	Output OD	HDMI_CTRL_CK	P105	I2C Clock line dedicated to HDMI. Connected to I2C2_CLK (1)
16	5V	IO OD	HDMI_CTRL_DAT	P106	I2C Data line dedicated to HDMI. Connected to I2C2_SDA (1)
17	GND	Power	CEC GND		Digital ground
18	5V	Power	5V HDMI		HDMI +5Volts
19	5V	Input	HDMI_HPD	P104	HDMI Hot Plug detect input. (1)
S1	GND	Power	GND		Digital ground
S2	GND	Power	GND		Digital ground
S3	GND	Power	GND		Digital ground
S4	GND	Power	GND		Digital ground
Notes					
(1)	These pins may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 23 HDMI connector signals

5.14 CSI: CAMERA SERIAL INTERFACE CONNECTORS

The BASE SMARC™ EXPANSION includes two MIPI-CSI2 connectors for MIPI-CSI2 cameras. In both cases, they are pin compatible with Raspberry Pi CS connector.

Next figures show connections for both CSI connectors (JCSI0 and JCSI1).

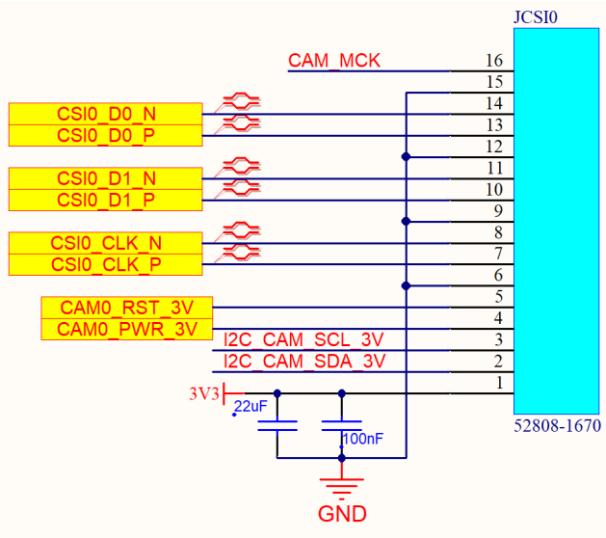


Figure 36 CSI0 connector schematics

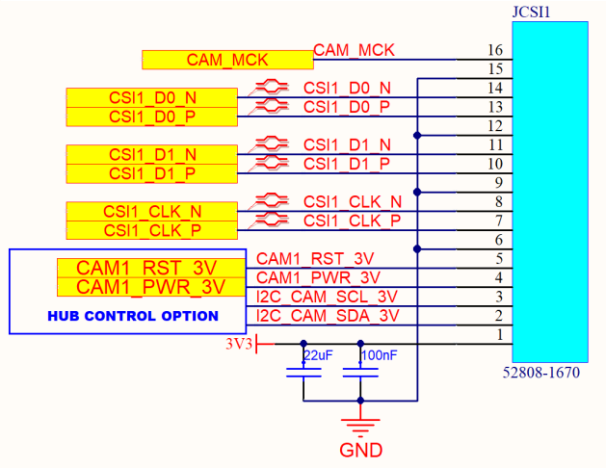


Figure 37 CSI1 connector schematics

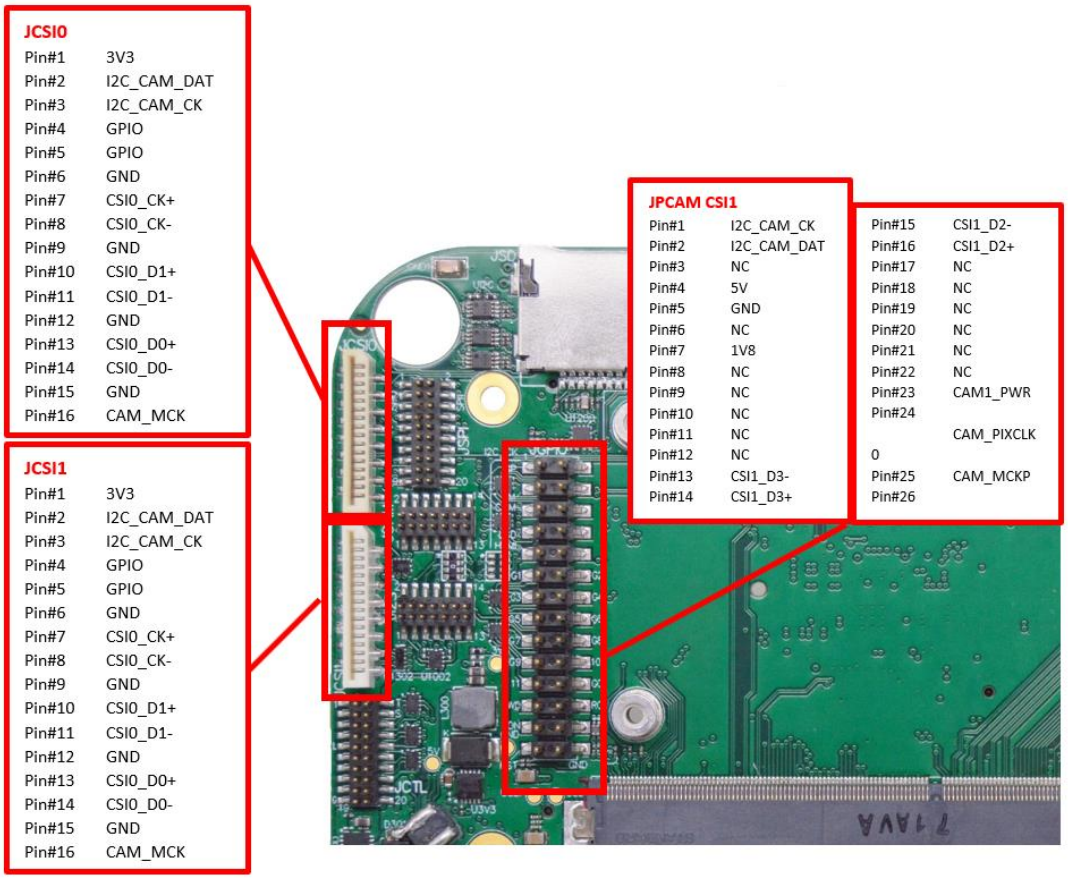


Figure 38 BASE SMARC™ EXPANSION: CSI – JCSI0, JCSI1 and JCAM connections

It is possible to expand CSI1 to four lanes. It can be done using the differential data input CSI1_D1 and CSI_D3 which can be found in the header JCAM.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JCSI0					
1	3V3	Power	3V3	3V3	Power Supply
2	3V3	IO OD	I2C_CAM_DAT	S7	I2C2: Data signal. (1)
3	3V3	IO OD	I2C_CAM_CK	S5	I2C2: Clock signal. (1)
4	3V3	IO	GPIO0	P108	General Purpose Input Output / CAM0 Power (1)
5	3V3	IO	GPIO2	P110	General Purpose Input Output / CAM0 Reset (Internal Enable-2 USB; Active High) (1)
6	GND	Power	GND	S3	Digital ground
7	LVDS D-PHY	Input	CSI0_CK+	S8	CSI differential Clock input.
8	LVDS D-PHY	Input	CSI0_CK-	S9	CSI differential Clock input.
9	GND	Power	GND	S10	Digital ground
10	LVDS D-PHY	Input	CSI0_D1+	S14	CSI D1 differential data input.

11	LVDS D-PHY	Input	CSI0_D1-	S15	CSI D1 differential data input.
12	GND	Power	GND	S13	Digital ground
13	LVDS D-PHY	Input	CSI0_D0+	S11	CSI D0 differential data input.
14	LVDS D-PHY	Input	CSI0_D0-	S12	CSI D0 differential data input.
15	GND	Power	GND	S16	Digital ground
16	1V8	Output	CAM_MCK	S6	Camera Master Clock
JCSI1					
1	3V3	Power	3V3		Power Supply
2	3V3	IO OD	I2C_CAM_DAT	S7	I2C2: Data signal. (1)
3	3V3	IO OD	I2C_CAM_CK	S5	I2C2: Clock signal. (1)
4	3V3	IO	GPIO1	P109	General Purpose Input Output / CAM1 Power (Internal Enable-1 USB; Active High) (1)
5	3V3	IO	GPIO3	P111	General Purpose Input Output / CAM1 Reset (Internal Enable-3 USB; Active High) (1)
6	GND	Power	GND	S3	Digital ground
7	LVDS D-PHY	Input	CSI1_CK+	P3	CSI differential Clock input.
8	LVDS D-PHY	Input	CSI1_CK-	P4	CSI differential Clock input.
9	GND	Power	GND	P9	Digital ground
10	LVDS D-PHY	Input	CSI1_D1+	P10	CSI D1 differential data input.
11	LVDS D-PHY	Input	CSI1_D1-	P11	CSI D1 differential data input.
12	GND	Power	GND	P12	Digital ground
13	LVDS D-PHY	Input	CSI1_D0+	P7	CSI D0 differential data input.
14	LVDS D-PHY	Input	CSI1_D0-	P8	CSI D0 differential data input.
15	GND	Power	GND	P15	Digital ground
16	1V8	Output	CAM_MCK	S6	Camera Master Clock
J5 - PARALLEL CAM CSI1					
1	1V8	IO	I2C_CAM1_CK	S1,S5	I2C2: Clock signal. Shared with I2C_CAM_CK
2	1V8	IO	I2C_CAM1_DAT	S1,S5	I2C2: Clock signal. Shared with I2C_CAM_DAT
3	NC	NC	NC	NC	NOT CONNECTED
4	5V	Power	5V		Power Supply
5	GND	Power	GND		Digital ground
6	NC	NC	NC	NC	NOT CONNECTED

7	1V8	Power	1V8		Power Supply
8	NC	NC	NC	NC	NOT CONNECTED
9	NC	NC	NC	NC	NOT CONNECTED
10	NC	NC	NC	NC	NOT CONNECTED
11	NC	NC	NC	NC	NOT CONNECTED
12	NC	NC	NC	NC	NOT CONNECTED
13	LVDS D-PHY	Input	CSI1_D3-	P17	CSI D3 differential data input.
14	LVDS D-PHY	Input	CSI1_D3+	P16	CSI D3 differential data input.
15	LVDS D-PHY	Input	CSI1_D2-	P14	CSI D2 differential data input.
16	LVDS D-PHY	Input	CSI1_D2+	P13	CSI D2 differential data input.
17	NC	NC	NC	NC	NOT CONNECTED
18	NC	NC	NC	NC	NOT CONNECTED
19	NC	NC	NC	NC	NOT CONNECTED
20	NC	NC	NC	NC	NOT CONNECTED
21	NC	NC	NC	NC	NOT CONNECTED
22	NC	NC	NC	NC	NOT CONNECTED
23	3V	Power	CAM1_PWR		Power Supply
24	1V8	Output	CAM_PIXCLK0	S4	Parallel Camera Pixel Clock 0
25	1V8	Output	CAM_MCKP	S6	Camera Master Clock
26	1V8	IO OD	PCAM_VSYNC	S1	I2C_CAM1_CK used to PCAM_VSYNC;
27	1V8	IO OD	PCAM_HSYNC	S2	I2C_CAM1_DAT used to PCAM_HSYNC;
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 24 CSI connector signals

5.15 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins to control LEDs, relays, switch, etc. The BASE SMARC™ EXPANSION has 12 GPIO lines to be configured by the user, placed in the JGPIO header. Please, be careful that in some cases these lines can be shared with other functions if they are present.

Next figure shows GPIO connector schematic.

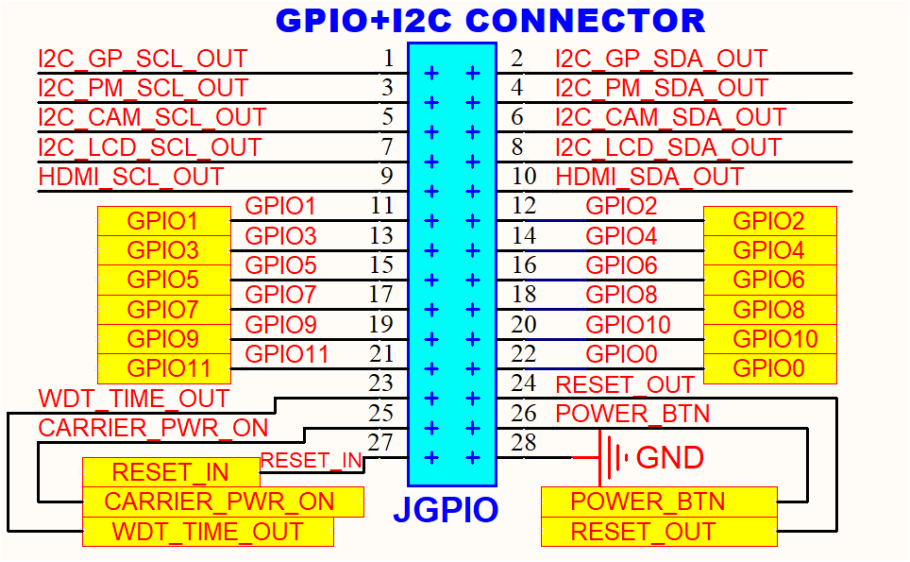


Figure 39 GPIO connector schematic

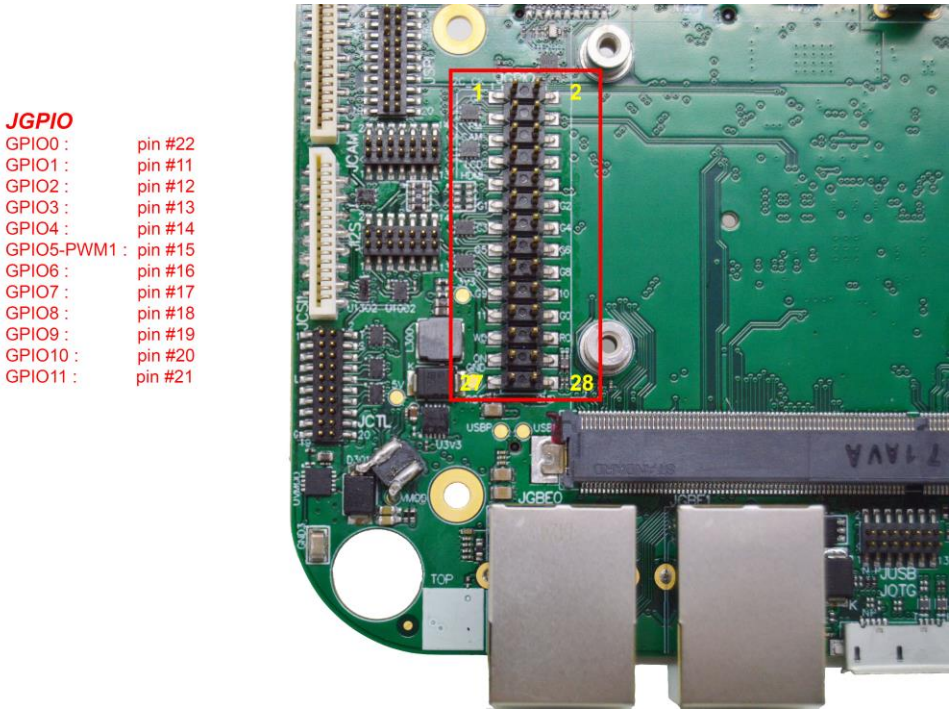


Figure 40 BASE SMARC™ EXPANSION:JGPIO – GPIO header

Next table shows the available GPIO signals in connector JGPIO.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JGPIO					
11	1V8	IO	GPIO1	P109	General Purpose Input Output / CAM1 Power (Internal Enable-1 USB; Active High)

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
12	1V8	IO	GPIO2	P110	General Purpose Input Output / CAM0 Reset (Internal Enable-2 USB; Active High)
13	1V8	IO	GPIO3	P111	General Purpose Input Output / CAM1 Reset (Internal Enable-3 USB; Active High)
14	1V8	IO	GPIO4	P112	General Purpose Input Output (Internal Reset CODEC; Active Low)
15	1V8	IO	GPIO5-PWM1	P113	General Purpose Input Output / PWM1
16	1V8	IO	GPIO6	P114	General Purpose Input Output (Internal Reset MODEM; Active High)
17	1V8	IO	GPIO7	P115	General Purpose Input Output (Internal SATA-PCIE_B Selection; Active High)
18	1V8	IO	GPIO8	P116	General Purpose Input Output (Internal SATA & MODEM LED W; Active High)
19	1V8	IO	GPIO9	P117	General Purpose Input Output (Internal USER_BUTTON, Active Low)
20	1V8	IO	GPIO10	P118	General Purpose Input Output (Internal DSI1_EN & USER_LED_BLUE; Active High)
21	1V8	IO	GPIO11	P119	General Purpose Input Output (USER_LED_RED; Active High)
22	1V8	IO	GPIO0	P108	General Purpose Input Output / CAM0 Power

Table 25 GPIO signals

5.16 PCIe INTERFACES

The BASE SMARCTM EXPANSION has four PCIe interfaces available. They are located in two mini-PICe connectors (JSATA and JMODEM) and in an expansion header (JPCIE).

PCI Interface	Connector
PCIE_A	JMODEM
PCIE_B	JSATA
PCIE_C PCIE_D	PCIE

Table 26 PCIe location interfaces

5.16.1 Interface PCIE_A and Modem

First interface is located in the mini-PCIe connector JMODEM and it is the defined in SMARC™ standard as PCIE_A. This connector is shared with a USB modem, which is using only the marked USB 2.0 Host signals indicated in pin table. As it is explained in chapter about USB 2.0 Host, there is used a Hi-Speed Hub controller which fourth port is used to stablish communications to GSM modem. To have the GSM communication it is also implemented a SIM-card connector (JSIM).

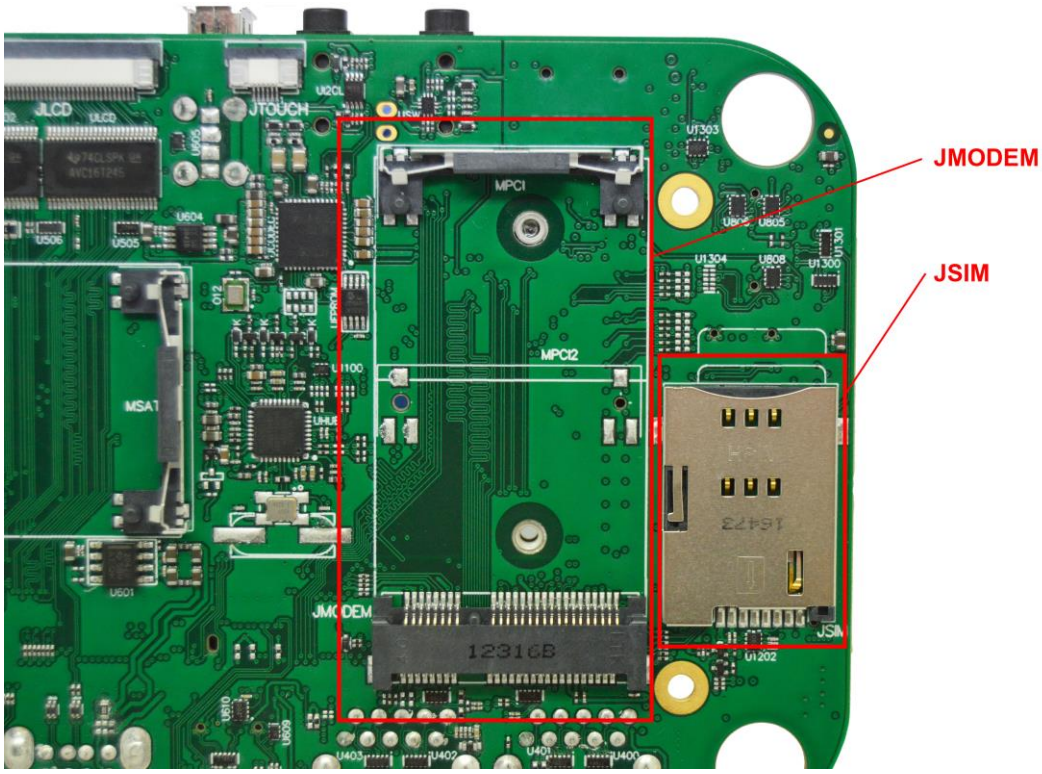


Figure 41 BASE SMARC™ EXPANSION: PCIE_A, Modem and SIM-Card – JMODEM & JSIM

5.16.2 Interface PCIE_B and mSATA

The second interface uses the other mini-PCIe connector (JSATA), which is also shared with the possibility to connect any kind of SATA device. This device uses only the SATA signals located in connector JSATA.

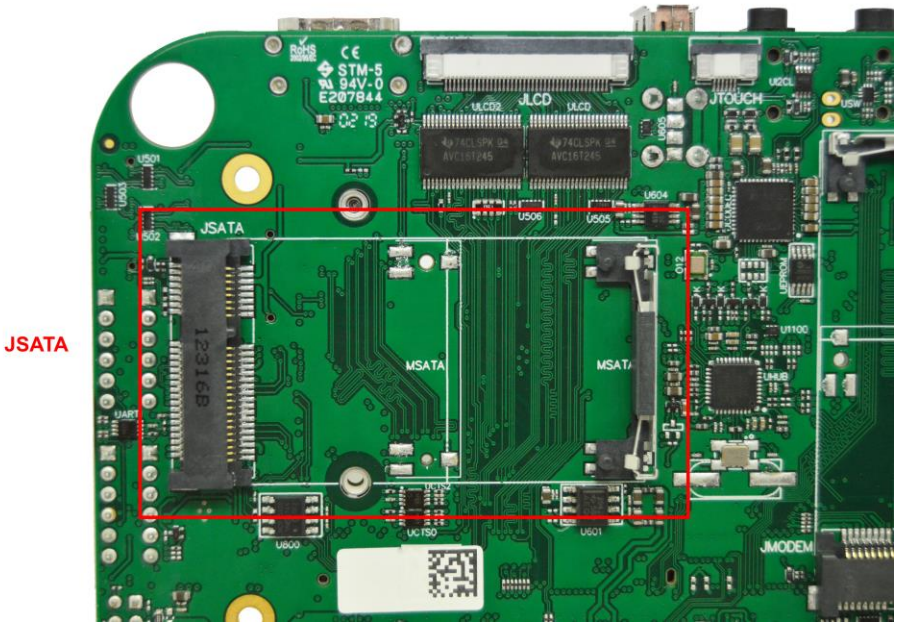
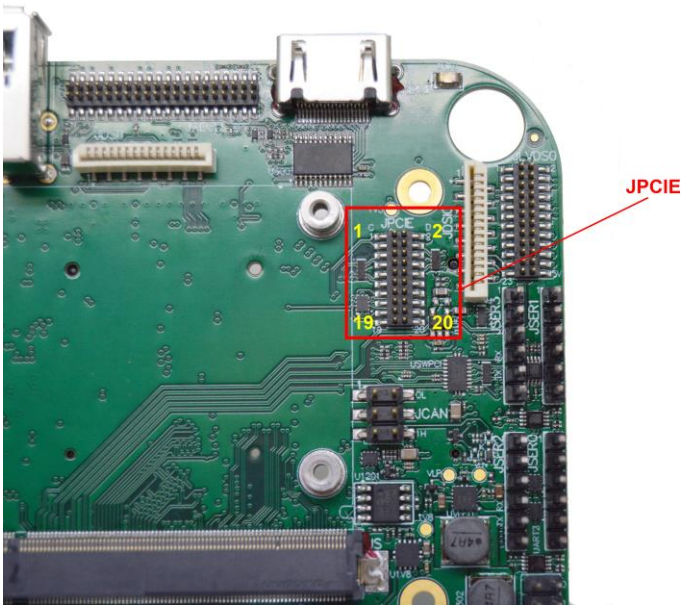


Figure 42 BASE SMARC™ EXPANSION:PCIE_C and PCIE_D - JPCIE

5.16.3 Interfaces PCIE_C and PCIE_D

The last two PCIe interfaces (PCIE_C and PCIE_D) are available in the JPCIE header.



Next table shows signals in connectors JPCIE, JSATA, JMODEM and JSIM.

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JPCIE					
1	PCIE	Output	PCIE_C_TX_N	S82	PCIE-C Transmitter Pair -
2	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
3	PCIE	Output	PCIE_C_TX_P	S81	PCIE-C Transmitter Pair +
4	PCIE	Output	PCIE_D_TX_N	S30	PCIE-D Transmitter Pair -
5	PCIE	Output	PCIE_C_RX_N	S79	PCIE-C Receiver Pair -
6	PCIE	Output	PCIE_D_TX_P	S29	PCIE-D Transmitter Pair +
7	PCIE	Output	PCIE_C_RX_P	S78	PCIE-C Receiver Pair +
8	PCIE	Output	PCIE_D_RX_N	S33	PCIE-D Receiver Pair -
9	PCIE	Output	PCIE_C_REFCK_N	P81	PCIE-C Reference Clock Pair -
10	PCIE	Output	PCIE_D_RX_P	S32	PCIE-D Receiver Pair +
11	PCIE	Output	PCIE_C_REFCK_P	P80	PCIE-C Reference Clock Pair +
12	1V8	Input	PCIE_C_PRSNTn	P72	PCIE-C Present (active Low)
13	3V3	Output	PCIE_C_RST#	S77	PCIE-C Reset (active Low)
14	1V8	IO	SATA_ACT	S54	GPIO2[13] (UART2_RTS)
15	3V3	Input	PCIE_C_CKREQ	P76	PCIE-C Clock Request (active Low)
16	3V3	Input	PCIE_A_PRSNTn	P74	PCIE-A Present (active Low)
17	NC	NC	NC	NC	Not connected
18	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
19	3V3	Input	PCIE_B_PRSNTn	P73	PCIE-B Present (active Low)
20	GND	Power	GND	P82	Digital ground
JMODEM					
1	3V3	Input	PCIE_WAKE#	S146	PCIe wake up interrupt to host
2	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
3	NC	NC	NC	NC	Not connected
4	GND	Power	GND	P120	Digital ground
5	NC	NC	NC	NC	Not connected

6	NC	NC	NC	1V5	(Internal 1V5 Power Supply)
7	3V3	Input	PCIE_A_CKREQ	P78	PCIE-A Clock Request (active Low)
8	1V8	Power	1V8	-	Internal 1V8 Power Supply. JSIM Power
9	GND	Power	GND	P133	Digital ground
10	1V8	IO	SIM DATA	-	SIM Card Data Line. Connected to JSIM
11	PCIE	Output	PCIE_A_REFCK_N	P84	PCIE-A Reference Clock Pair -
12	1V8	Output	SIM CLK	-	SIM Card Clock Line. Connected to JSIM
13	PCIE	Output	PCIE_A_REFCK_P	P83	PCIE-A Reference Clock Pair +
14	1V8	Output	SIM RESET	-	SIM Card Reset Line. Connected to JSIM
15	GND	Power	GND	P120	Digital ground
16	NC	NC	NC	NC	Not connected
17	NC	NC	NC	NC	Not connected
18	GND	Power	GND	P50	Digital ground
19	NC	NC	NC	NC	Not connected
20	3V3	Output	WDIS	-	Fixed to Low Level
21	GND	Power	GND	S92	Digital ground
22	3V3	IO	GPIO6	P114	General Purpose Input Output (Internal Reset MODEM; Active High)
22	3V3	Output	PCIE_A_RST#	P75	PCIE-A Reset (active Low)
23	PCIE	Output	PCIE_A_RX_N	P87	PCIE-A Receiver Pair -
24	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
25	PCIE	Output	PCIE_A_RX_P	P86	PCIE-A Receiver Pair +
26	GND	Power	GND	S89	Digital ground
27	GND	Power	GND	P59	Digital ground
28	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
29	GND	Power	GND	P68	Digital ground
30	3V3	IO OD	I2C_CAM1_CK	S1,S5	I2C2: Clock signal. Shared with I2C_CAM_CK

31	PCIE	Output	PCIE_A_TX_N	P90	PCIE-A Transmitter Pair -
32	3V3	IO OD	I2C_CAM1_DAT	S2,S7	I2C2: Data signal. Shared with I2C_CAM_DAT
33	PCIE	Output	PCIE_A_TX_P	P89	PCIE-A Transmitter Pair +
34	GND	Power	GND	P79	Digital ground
35	GND	Power	GND	P82	Digital ground
36	USB	IO	USB1-	P66	UBS1: USB2.0 differential data input. USB-HUB-4
37	GND	Power	GND	P85	Digital ground
38	USB	IO	USB1+	P65	UBS1: USB2.0 differential data input. USB-HUB-4
39	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
40	GND	Power	GND	P88	Digital ground
41	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
42	3V3	IO	LEDWW	P116	GPIO8. Internal SATA & MODEM LED W; Active High
43	GND	Power	GND	P94	Digital ground
44	3V3	IO	LEDWL	P116	GPIO8. Internal SATA & MODEM LED W; Active High
45	1V8	IO	I2S1_CK	S46	I2S1 Digital Audio BIT clock.
46	3V3	IO	LEDWP	P116	GPIO8. Internal SATA & MODEM LED W; Active High
47	1V8	Output	I2S1_SDOUT	S44	I2S1 Digital Audio output.
48	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
49	1V8	Input	I2S1_SDIN	S45	I2S1 Digital Audio input.
50	GND	Power	GND	P91	Digital ground
51	1V8	IO	I2S1_SYNC	S43	I2S1 Left & Right Audio synchronization clock.
52	3V3	Power	3V3	-	Internal 3V3 Power Supply for Modem
JSATA					
1	3V3	Input	PCIE_WAKE#	S146	PCIe wake up interrupt to host
2	3V3	Power	3V3	-	Internal 3V3 Power Supply
3	NC	NC	COEX1	NC	No connected
4	GND	Power	GND	P120	Digital ground

5	NC	NC	COEX2	NC	Not connected
6	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
7	3V3	Input	PCIE_B_CKREQ	P77	PCIE-B Clock Request (active Low)
8	NC	NC	SIM PWR	NC	SIM POWER. Not connected
9	GND	Power	GND	P133	Digital ground
10	NC	NC	SIM DATA	NC	SIM Card Data Line. Not connected
11	PCIE	Output	PCIE_B_REFCK_N	S85	PCIE-B Reference Clock Pair -
12	NC	NC	SIM CLK	NC	SIM Card Clock Line. Not connected
13	PCIE	Output	PCIE_B_REFCK_P	S84	PCIE-B Reference Clock Pair +
14	NC	NC	SIM RESET	NC	SIM Card Reset Line. Not connected
15	GND	Power	GND	S86	Digital ground
16	NC	NC	SIM VDD	NC	Not connected
17	NC	NC	NC	NC	Not connected
18	GND	Power	GND	P50	Digital ground
19	NC	NC	NC	NC	Not connected
20	3V3	Output	WDIS	-	Fixed to Low Level
21	GND	Power	GND	S92	Digital ground
22	3V3	Output	PCIE_B_RST#	S76	PCIE-B Reset (active Low)
23	PCIE	Output	PCIE_B_RX_N	S88	PCIE-B Receiver Pair -
23	SATA	Output	SATA_RX+	P51	SATA_RX+ Sata Pair RX
24	3V3	Power	3V3	-	Internal 3V3 Power Supply
25	PCIE	Output	PCIE_B_RX_P	S87	PCIE-B Receiver Pair +
25	SATA	Output	SATA_RX-	P52	SATA_RX- Sata Pair RX
26	GND	Power	GND	S89	Digital ground
27	GND	Power	GND	P59	Digital ground
28	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
29	GND	Power	GND	P68	Digital ground
30	3V3	IO OD	I2C_CAM1_CK	S1,S5	I2C2: Clock signal. Shared with I2C_CAM_CK

31	PCIE	Output	PCIE_B_TX_N	S91	PCIE-B Transmitter Pair -
31	SATA	Output	SATA_TX-	P49	SATA_TX- Sata Pair TX
32	3V3	IO OD	I2C_CAM_DAT	S7	I2C2: Data signal. Shared with
33	PCIE	Output	PCIE_B_TX_P	S90	PCIE-B Transmitter Pair +
33	SATA	Output	SATA_TX+	P48	SATA_TX+ Sata Pair TX
34	GND	Power	GND	P79	Digital ground
35	GND	Power	GND	P82	Digital ground
36	NC	NC	NC	NC	Not connected
37	GND	Power	GND	P85	Digital ground
38	NC	NC	NC	NC	Not connected
39	3V3	Power	3V3	-	Internal 3V3 Power Supply
40	GND	Power	GND	P88	Digital ground
41	3V3	Power	3V3	-	Internal 3V3 Power Supply
42	3V3	IO	LEDWW	P116	GPIO8. Internal SATA & MODEM LED W; Active High
43	3V3	IO	SATA-PCIE	P115	GPIO7. Internal SATA-PCIE_B Selection; Active High
44	3V3	IO	LEDWL	P116	GPIO8. Internal SATA & MODEM LED W; Active High
45	NC	NC	NC	NC	Not connected
46	3V3	IO	LEDWL	P116	GPIO8. Internal SATA & MODEM LED W; Active High
47	NC	NC	NC	NC	Not connected
48	1V5	Power	1V5	-	(Internal 1V5 Power Supply)
49	1V8	IO	SATA_ACT	S54	GPIO2[13] (UART2_RTS)
50	GND	Power	GND	P91	Digital ground
51	3V3	Input	3V3	-	PCIE-B Present (active Low)
52	3V3	Power	3V3	-	Internal 3V3 Power Supply
JSIM					
1	1V8	Power	SIM POWER	-	Internal 1V8 Power Supply. JSIM Power
2	GND	Power	GND		Digital ground
3	1V8	IO	SIM RESET	-	SIM Card Reset Line. Connected to JSIM
4	NC	NC	NC	NC	Not connected

5	1V8	IO	SIM CLK	-	SIM Card Clock Line. Connected to JSIM
6	1V8	IO	SIM DATA	-	SIM Card Data Line. Connected to JSIM
7	NC	NC	NC	NC	Not connected
8	GND	Power	GND		Digital ground
9	GND	Power	GND		Digital ground
10	GND	Power	GND		Digital ground

Table 27 PCIe signals

5.17 CAN BUS: CONTROLLER AREA NETWORK

The BASE SMARC™ EXPANSION offers the possibility to integrate the IGEP™ SMARC™ processors family (if this function is available on that model) to a serial CAN bus. This is available through the header JCAN and there are up to two CAN bus connections.

Next figure shows the CAN bus connections.

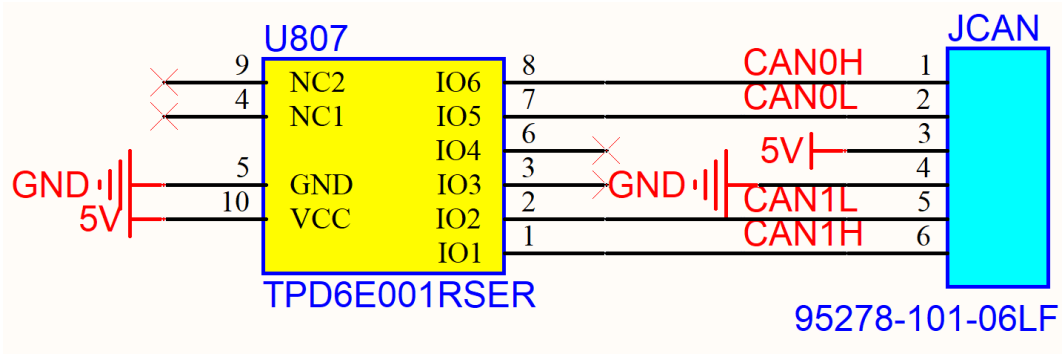


Figure 43 CAN Bus schematic

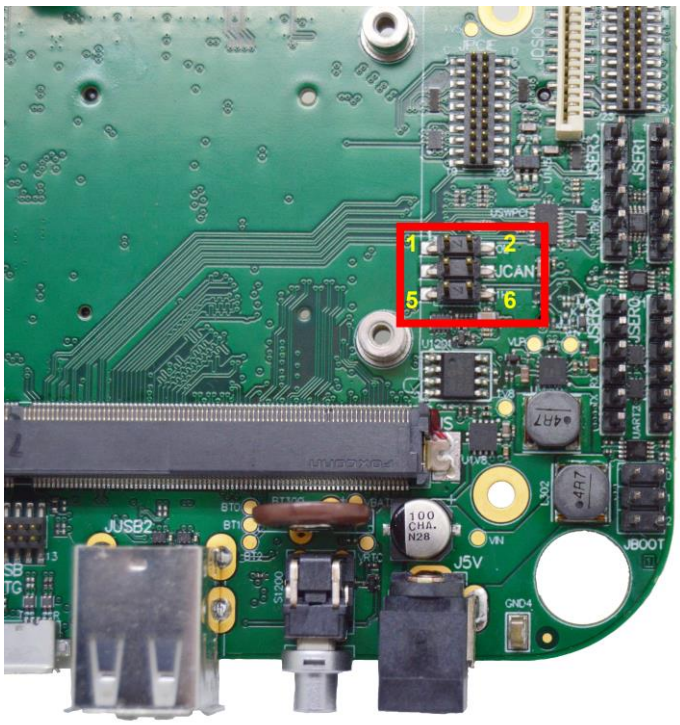


Figure 44 BASE SMARC™ EXPANSION: JCAN – CAN Bus header

Connector Pin	Volt Level	Type	Function	JSMARC	Comments
JCAN					
1	5V	Output	CAN0_TX	P143	CAN0 Transmitter Line (1)
2	5V	Input	CAN0_RX	P144	CAN0 Receiver Line (1)
3	5V	Power	VDD_IN	P147	Pins used to power up the module. 4,75 V to 5,25 V
4	GND	Power	GND	P142	Digital ground
5	5V	Input	CAN1_RX	P146	CAN1 Receiver Line (1)
6	5V	Output	CAN1_TX	P145	CAN1 Transmitter Line (1)
Notes					
(1)	This pin may not be directly connected to the corresponding pin on JSMARC, there could be a level translator in between.				

Table 28 CAN Bus signals

5.18 RTC BATTERY

There is also included a backup battery (VBAT) that powers the backup state as far as the input voltage is high enough. It is used a lithium ion rechargeable battery 3 V with 7 mAh capacity (VL1220-1VC).

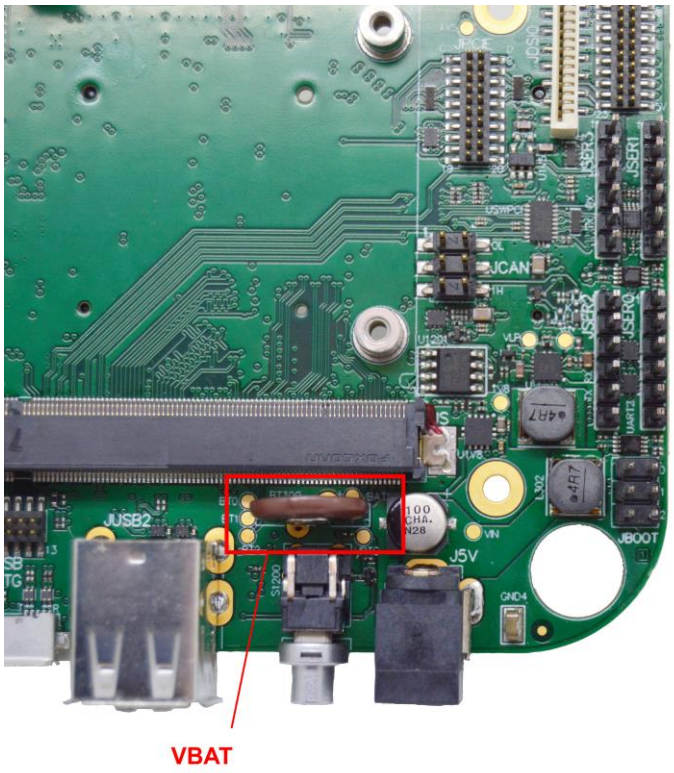


Figure 45 BASE SMARC™ EXPANSION: VBAT-RTC Battery

The Carrier Board have implemented the needed circuits to protect against charging by reverse currents.

Pin	Volt Level	Type	Main Function	Comments
S147	3V	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.

Table 29 RTC pin

5.19 ENVIRONMENTAL SPECIFICATION

General Specification	Operating	Non-operating
Industrial grade (E2)	-40ºC to +80ºC	-40ºC to +80ºC

Table 30 Temperature range

Standard modules are available for Industrial grade temperature range. The operating temperature is the maximum measurable temperature on any spot on the module's surface.

- **Humidity**

93% relative Humidity at 40ºC, non-condensing (according to IEC 60068-2-78).

5.20 STANDARDS AND CERTIFICATIONS

- **RoHS**

The SMARC™ Expansion is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

- **CE Marking**

The SMARC™ Expansion is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

- **WEEE Directive**

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

- **Conformal Coating**

Conformal Coating is available for Computer-on-Modules and for validated SMARC modules. Please, contact your local sales or support for further details.

- **EMC**

The SMARC Expansion is designed and tested following EN55022 standard (“INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT”).

- **SMARC Form Factor standard**

The SMARC ("Smart Mobility Architecture") is a versatile small form factor computer Module definition targeting application that require low power, low costs and high performance.

5.21 MECHANICAL SPECIFICATION

- **Base Dimension**
  - 142,00 mm x 90,00 mm x 4,30 mm
  - Case dimensions: 150,00 mm x 100,00 mm x 30,00 mm

- **Mechanical Drawing**

The next figures show the BASE SMARC™ EXPANSION board mechanical dimensions:

- All dimensions are in millimeters.
- 8-layer Printed Circuit Board size is 142,00 mm x 90,00 mm x 1,15 mm.
- Mounting holes are provided, one on each corner.

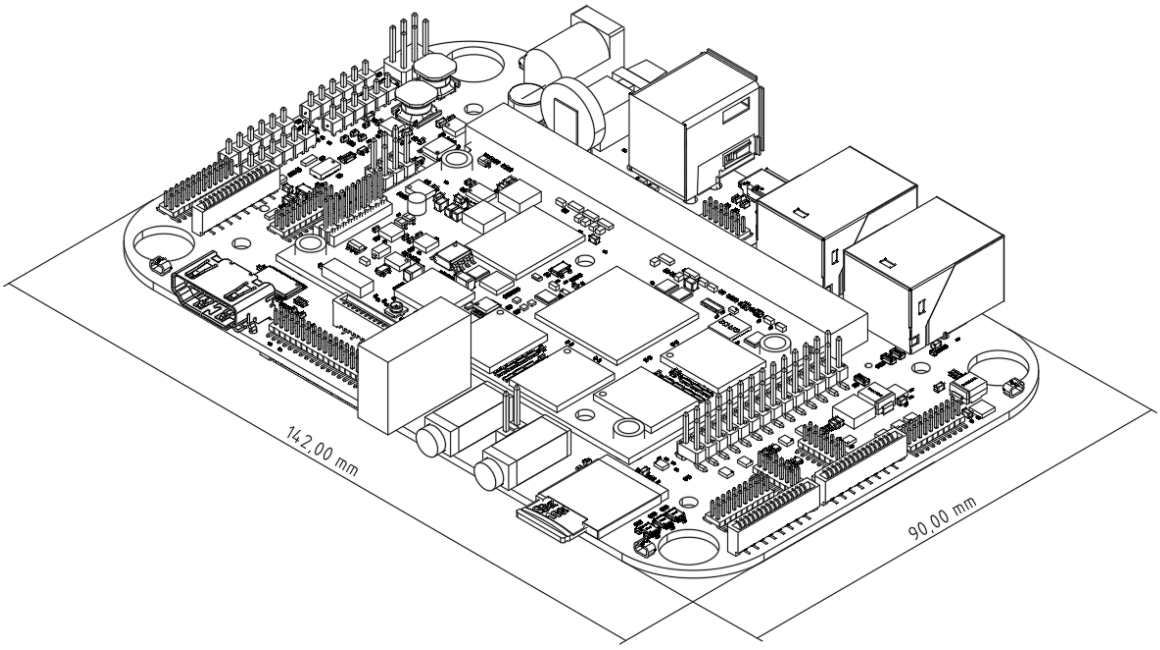


Figure 46 BASE SMARC™ EXPANSION Outline dimensions

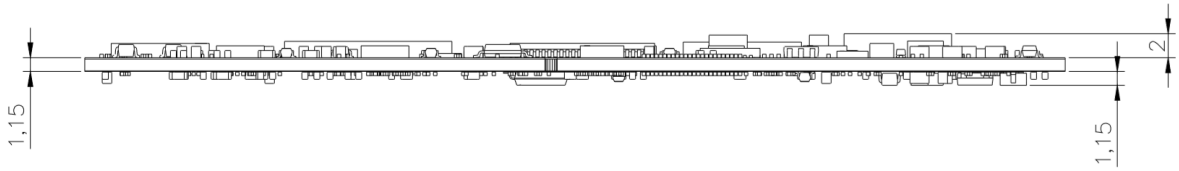


Figure 47 BASE SMARC™ EXPANSION Lateral view widths dimensions

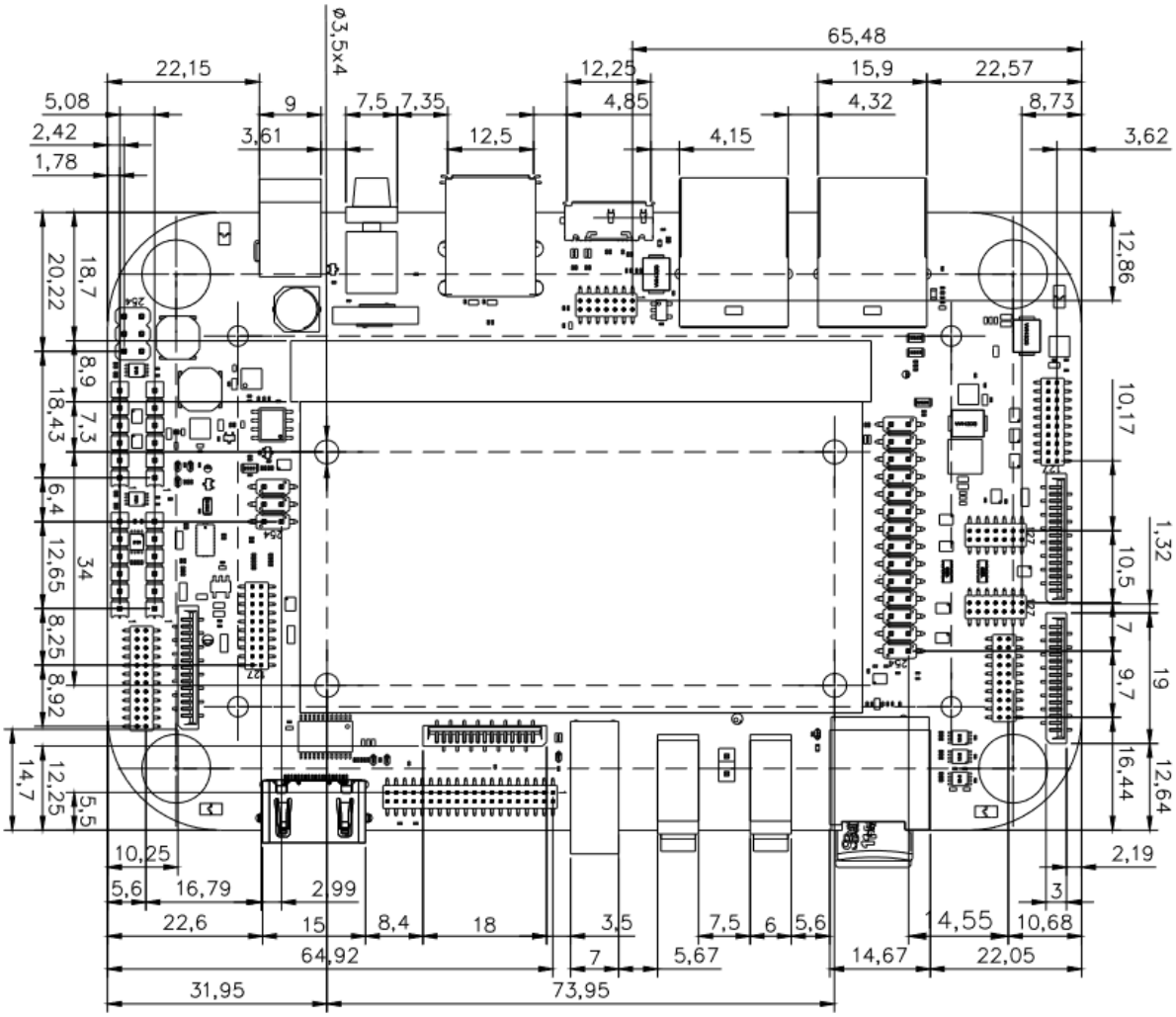


Figure 48 BASE SMARC™ EXPANSION Side view detailed mechanical dimension

6 ELECTRICAL CHARACTERISTICS

All electrical characteristics pins are stablished by SMARC™ specification.

Electrical parameter	Min	Typ	Max	Unit
5 V INPUT POWER SUPPLY				
BASE IGEP™ SMARC EXPANSION Input Power Supply Voltage	3.0	-	5.25	V
BASE IGEP™ SMARC EXPANSION Input Power Supply Current (1)	-	0.13	4	A
Input/Output pins				
Output High-Level DC Voltage (1)	1.6	1.8	2.1	V
Input High-Level DC Voltage (1)	1.26	1.8	2.1	V
Output Low-Level DC Voltage (1)	-	-	0.2	V
Input Low-Level DC Voltage (1)	0	-	0.54	V
RTC_BATTERY type pins				
Input DC Voltage	2.5	3	3.25	V
USB type pins				
Input/Output High-Level DC Voltage	4.75	5	5.25	V
Output Drive Current	0	500	500	mA

Table 31 BASE IGEP™ SMARC EXPANSION Electrical Characteristics

(1) The electrical specification depends on the selected IGEP SMARC™ module to use.

BASE SMARC™ EXPANSION AND CONNECTED MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED.

WARRANTY LOST IF IMPROPER USE OF THE BASE OR MODULE IS FOUND.

7 Document and Standards References

- **CAN** (“Controller Area Network”) Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- **MIPI CSI-2** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **MIPI CSI-3** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **COM Express** – the formal title for the COM Express specification is “PICMG® COM.0 COM Express Module Base Specification”, Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG (“PCI Industrial Computer Manufacturer’s Group”) (www.picmg.org)
- **DisplayPort and Embedded DisplayPort -** These standards are owned and maintained by VESA (“Video Electronics Standards Association”) (www.vesa.org)
- **MIPI DSI** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **eMMC** (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- **eSPI** (“Enhanced Serial Peripheral Interface”) The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- **Fieldbus** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: https://www.profibus.com/download/ and www.can-cia.org
- **GBE MDI** (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **HDA (HD Audio),** High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (http://www.intel.com)
- **HDMI Specification,** Version 2.1, November 28, 2017 (www.hdmi.org)
- **I2C Specification,** Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (www.nxp.com)
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- **IEEE1588 - 2008**. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (http://standards.ieee.org)
- **JTAG** (“Joint Test Action Group”) This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (https://ieeexplore.ieee.org)
- **MXM3** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- **PICMG® EEEP** Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org)
- **PCI Express** Specifications (www.pci-sig.org)
- **Serial ATA** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org) SMARC 2.1.1 Specification © 2020 SGET e.V. Page 9 of 109
- **SD Specifications** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)
- **SM Bus** – “System Management Bus” Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (http://www.smbus.org)

- **SPI Bus** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- **USB** Specifications (http://www.usb.org)