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IGEP™ TECHNOLOGY

IGEP™ SMARC iMX8M

HARDWARE REFERENCE MANUAL

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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1 USER INFORMATION

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2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The IGEP™ SMARC iMX8M is an industrial ultra-low computer module based on iMX8M processor family by NXP, featuring and ARM Cortex-A53 (with a speed of 1300 MHz) and an additional 266 MHz ARM Cortex-M4 core.

This multicore processing architecture enables to run a Linux operating system with main application on the Cortex-A53, using the Cortext-M4 core for time and security critical tasks.

It's an industrial computer module (it can work in a temperature range from -40ºC to +85ºC), in a very low profile according the standard form factor SMARC by SGET (its size is only 82,00 mm x 50,00 mm). With different combinations of RAM and Flash memory (see customized possibilities at chapter 2.4) and a complete list of interfaces and peripherals including 3D graphic accelerator, it can be the base for a complex industrial equipment or any other kind of application.

For development purposes there is also available an expansion board (IGEP™ SMARC EXPANSION) to complete the module. It can be used as the fastest way to develop the user's final application before the prototyping phase. This expansion board can be used with all IGEP™ SMARC modules.

Highlights:

- Fully tested, highly reliable, scalable, efficient and high performing board that allows customers to focus on their end application.
- Designed for industrial range purposes (temperature range: -40ºC to +85ºC).
- Form factor according to small size SMARC (82,00 mm x 50,00 mm).
- Easy connectivity through MXM3 graphic cards type connector: 314-pin, 0,5 pitch right angle.
- 1V8 I/O level digital signals.
- JTAG interface available.
- Based on NXP iMX8M processor, with Quad core ARM Cortex-A53 and a Low Power co-processor ARM Cortex-M4 at 266 MHz.
- 10/100/1000 Mbps Ethernet MAC+PHY interface.
- Flexible Flash Memory combinations (customized option).
- WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity
- RAM memory size: Up to 4 GB LPDDR4.
- Flash memory size: Up to 64 GB eMMC.
- Low Power solution.
- Compatible with SMARC modules.

2.2 IGEP™ SMARC iMX8M BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ SMARC iMX8M series. Reducing the implementation time and saving costs on their designs. Amongst others, the main benefits are the following:

- Easy scalability between different modules (even with other processors) thanks to the SMARC standard.
- Compact and powerful core for new products.
- Robust and easy to mount due to the MXM3 314-pin connector.
- Reduced time to market.
- Low power consumption: Typical 3W (room temperature 25ºC, using heatsink and 50% load).
- Industrial Temperature Range -40 to +85ºC.
- Extended life range product.

At the same time, it can be implemented in all kind of end applications. The followings are just a few ones, but the list can be as long as the imagination of the developers.

- Connected vending machines.
- Home / Building automation (IoT applications).
- Human Interface.
- Industrial Control.
- Test and Measurement.
- Artificial Intelligence

2.3 SMARC STANDARD

The IGEP™ SMARC iMX8M accomplish the SMARC 2.0 version, which is defined by SGET.

The SMARC (“Smart Mobility Architecture”) is a computer Module definition targeting applications that require low power, low costs, and high performance. This standard is based on the former ULP-COM standard (Ultra Low Power Computer-on-Modules). The Modules will typically use ARM SoCs (System on Chip) families or similar.

SMARC standard defines two module sizes (82mm x 50mm and 82mm x 80mm). **All the available IGEP modules sizes 82mm x 50mm**. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin (156 on TOP side and 158 on BOTTOM side) right angle connector. The module pins are designated as P1-P156 on the TOP side and S1 – S158 on the BOTTOM side. The connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key (4 on the TOP side and 3 on the BOTTOM side).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

2.4 SMARC FORM FACTOR FEATURE SUMMARY

Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards.
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out.
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom)
    - Other stack height options available, including 2.7mm, 5mm, 8mm
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector.
- Module input voltage range: 3.0V to 5.25V
  - Allows operation from 3.6V nominal Lithium-ion battery packs.
  - Allows operation from 3.3V fixed DC supply.
  - Allows operation from 5.0V fixed DC supply.
  - Single supply (no separate standby voltage).
  - Module power pins allow 5A max.
- Low power designs
  - Fanless
  - Passive cooling
  - Low standby power
  - Design for battery operation
  - 1.8V default I/O voltage

2.5 MODULE INTERFACE SUMMARY

The interfaces listed below are available per the Module pin definition.

- Display Interfaces
  - Single LVDS LCD 24 bit
  - HDMI port multiplexed with DP++ full featured implementation
  - Additional full featured DisplayPort++
- Camera Interfaces
  - Two Serial configuration: MIPI CSI (4 lane)
- SDIO Interface
  - 4 bit SD card / SDIO interface with support lines
- SPI Interfaces
  - One SPI interfaces
- Audio Interfaces
  - Up to three I2S interface

- I2C Interfaces
  - Four I2C interfaces
    - Power Management
    - General Purpose
    - 2x Camera Interfaces
    - LCD Display ID
  - HDMI interface also has private I2C interface for HDMI use
- Asynchronous Serial Port Interfaces
  - Four asynchronous serial ports
    - Two supporting 2 wire handshake (RXD, TXD, RTS#, CTS#)
    - Two supporting data only (RXD, TXD)
- USB Interfaces
  - Two sets of super speed signals for support of two USB 3.0 ports
    - One Port supporting USB OTG
    - One Port supporting USB Host
  - USB support signals (VBUS enable / Over-current detects, OTG support signals)
- PCI Express
  - Two PCIe lanes
  - Two reference clock pairs
  - Two PCIe reset signals
  - Common PCIe wake signal (PCIE_WAKE#)
  - Two PCIE_CKREQ# signals for PCIE_A and PCIE_B
- Gigabit Ethernet
  - Two analog GBE MDI interface
  - No magnetics on Module
  - LED support signals
  - CTREF (center tap reference voltage) for Carrier magnetics (if required by the Module GBE PHY)
  - Individual IEEE1588 trigger signal for each Ethernet interface to allow for enhanced real time applications. This utilizes a software definable pin (SDP) from the Ethernet controller.
- Wireless
  - Optional on module wireless functionality with designated area for antenna connections
- Watchdog Timer Interface
- General Purpose I/O
  - 12x GPIO signals
- System and Power Management Signals
  - Reset out and Reset in
  - Power button in
  - Power source status
  - Module power state status
  - System management pins
  - Carrier Power On control
- Boot Source Select
  - Three pins to allow selection from Carrier Board
  - Select options to include boot from one of the following:
    - Module eMMC Flash
    - Module Remote Boot (Network (GBE) or Serial Port
    - Carrier SD Card
- JTAG functions for CPU debug and test are optionally implemented on separate small form factor connector

2.6 IGEP™ SMARC iMX8M SERIES

The IGEP™ SMARC iMX8M series is composed by Quad core processor and different memory configuration.

IGEP™ SMARC iMX8M-Quad is composed by a Quad Cortex-A53 Core 1,3 GHz and a 266 MHz ARM Cortex-M4, with 3 GB LPDDR4 RAM memory and 8 GB eMMC Flash memory. The standard version is manufactured with WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity.

Other combinations are available. Contact with IATEC's Sales Department for other configurations.

2.7 PARTS NUMBERS

Depending on the module configuration, the module has different parts numbers.

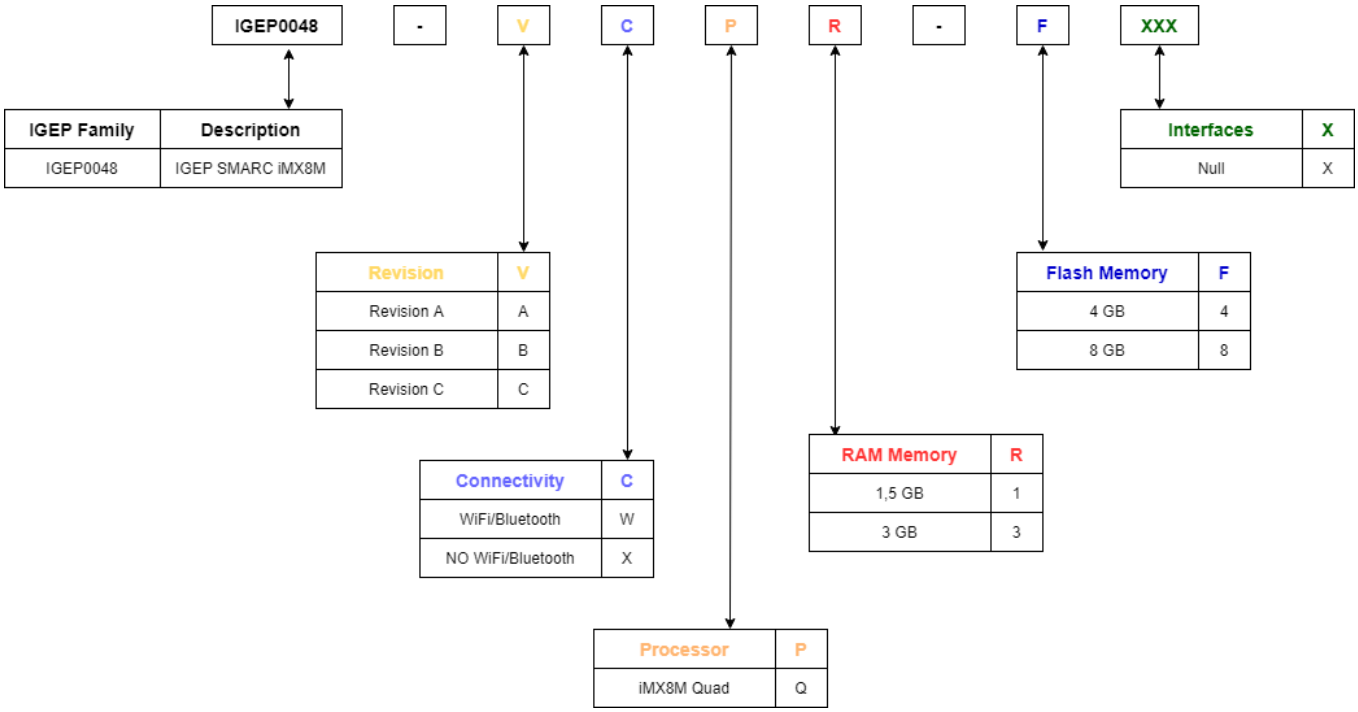

Figure 1 IGEP™ SMARC iMX8M Possible Part Number

Part Number	IGEP™ Device	Description
IGEP0048-BWQ1-4XXX	SMARC iMX8M-Quad WiFi	Processor: iMX8M-Quad RAM Memory: LPDDR4 1,5 GB Flash Memory: eMMC 4 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2
IGEP0048-BXQ1-4XXX	SMARC iMX8M-Quad No WiFi	Processor: iMX8M-Quad RAM Memory: LPDDR4 1,5 GB Flash Memory: eMMC 4 GB
IGEP0048-BWQ3-8XXX	SMARC iMX8M-Quad WiFi	Processor: iMX8M-Quad RAM Memory: LPDDR4 3 GB Flash Memory: eMMC 8 GB Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2
IGEP0048-BXQ3-8XXX	SMARC iMX8M-Quad No WiFi	Processor: iMX8M-Quad RAM Memory: LPDDR4 3 GB Flash Memory: eMMC 8 GB

Table 1 IGEP™ SMARC iMX8M Ordering Information.

3 HARWARE OVERVIEW

3.1 IGEPTM SMARC iMX8M

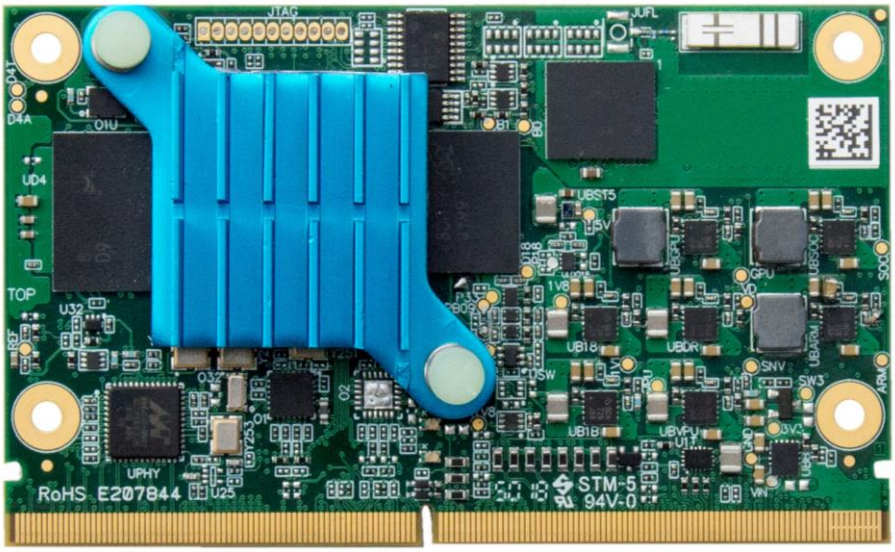

Figure 2 SMARC iMX8M – Top View

Figure 3 SMARC iMX8M – Bottom View

3.2 IGEP™ SMARC iMX8M BLOCK DIAGRAM

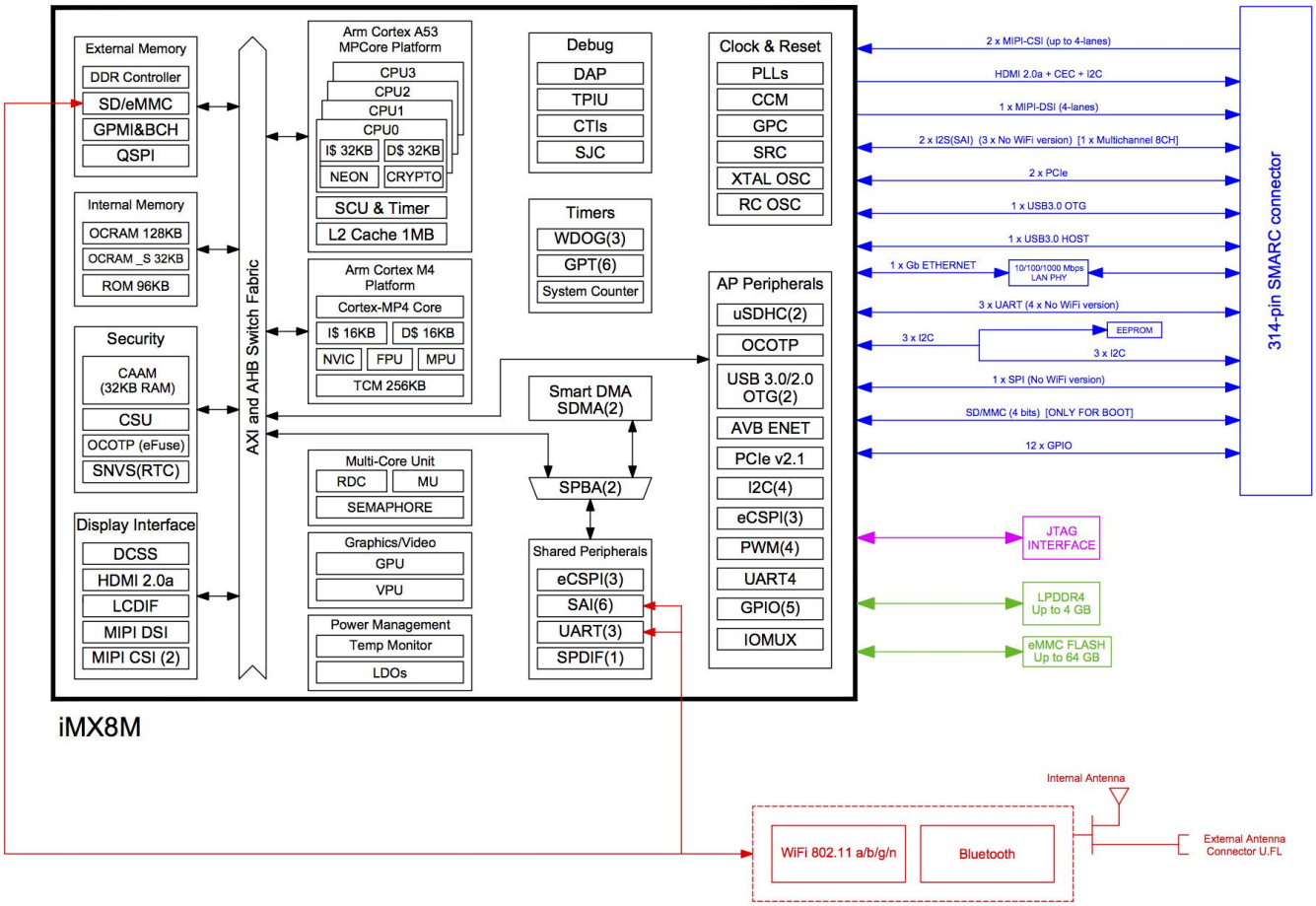

Figure 4 IGEP™ SMARC iMX8M Block Diagram

3.3 IGEP™ SMARC iMX8M FEATURES

Feature	Specifications
Processor	NXP iMX8M Quad 2 or 4 x ARM Cortex-A53 Frequency: 1,3 GHz Low Power co-processor: Cortex-M4 @266 MHz
Memory	RAM: 1 to 4 GB LPDDR4 Flash: 4 to 64 eMMC EEPROM: Serial I2C 32 Kb
3D/2D Graphics Accelerator	GPU: Vivante GC7000Lite Support: OpenGL ES 3.0, Open GL 3.0, OpenCL 1.2, OpenVG 1.0, Vulkan, EGL 1.4, DirectX 11
Video	Decode: 4Kp60 with High Dynamic Range (H.265, VP9), 4Kp30 (H.264), 1080p60 (MPEG2, MPEG4p2, VC1, VP8, AVS/AVS+, H.263, DivX), MJPEG
Camera Interface	2 x MIPI-CSI, 4-lanes
Display	HDMI: 2.0a up to 4K 60p DSI: 1920x1080p60, 4-lanes
Digital Audio	2 x I2S(SAI) (No WiFi versions: 3x)
Network	Ethernet: 10/100/1000 Mbps WiFi: Certified 802.11 b/g/n (Access Point: Yes) Bluetooth: 4.2
Antenna	Internal WiFi/Bluetooth antenna Optional: U.FL connector for external antenna
USB	1 x USB 3.0 Host/OTG 1 x USB 2.0 Host
External Interfaces	3x UART (No WiFi versions: 4x) 1 x SD/MMC (only in Boot for WiFi version) 4x I2C 1 x SPI 2 x PCIe v2.0 12 x GPIO 1 x JTAG
OS Support	Linux Kernel 4.9 Distributions: Ubuntu 16.04, Yocto 2.3, Debian
Power Supply	Power from expansion connectors: From 3,0 V to 5,25 V Digital I/O voltage: 1,8 V
Power Consumption	0.43 A
Thermal	Industrial temperature: -40ºC to +80ºC
Form Factor	Small SMARC size: 82,00 mm x 50,00 mm
Humidity	93% relative Humidity at 40 ºC, non-condensing (according to IEC 60068-2-78)
MTBF	131400 hours (>15 years)

Table 2 On-board features

3.4 IGEP™ SMARC iMX8M COMPONENTS MAP

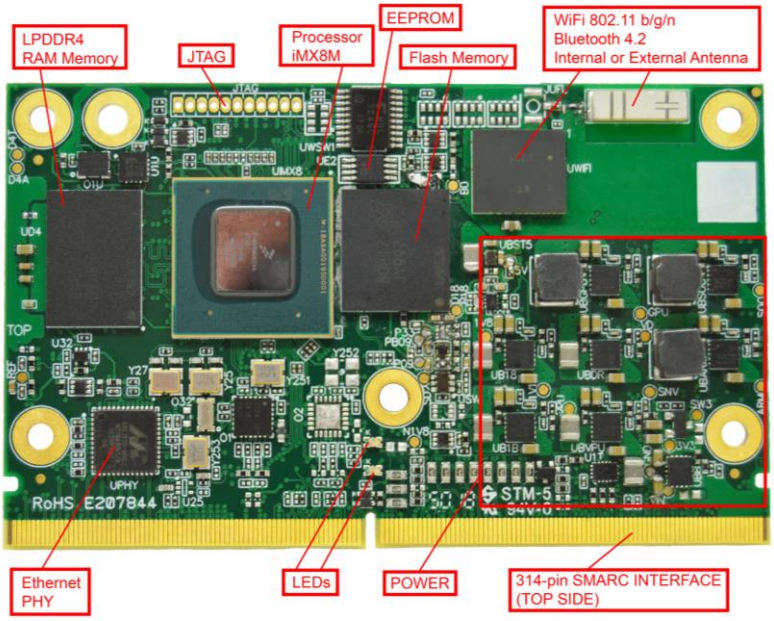

Figure 5 SMARC iMX8M Components Map

3.5 NXP iMX8M PROCESSORS

The iMX8M by NXP are a family of highly integrated processors based on the ARM Cortex-A53 processor with frequency speed of 1,3 GHz (in Industrial version). This is complemented of a low power co-processor Cortex-M4 at 266 MHz.

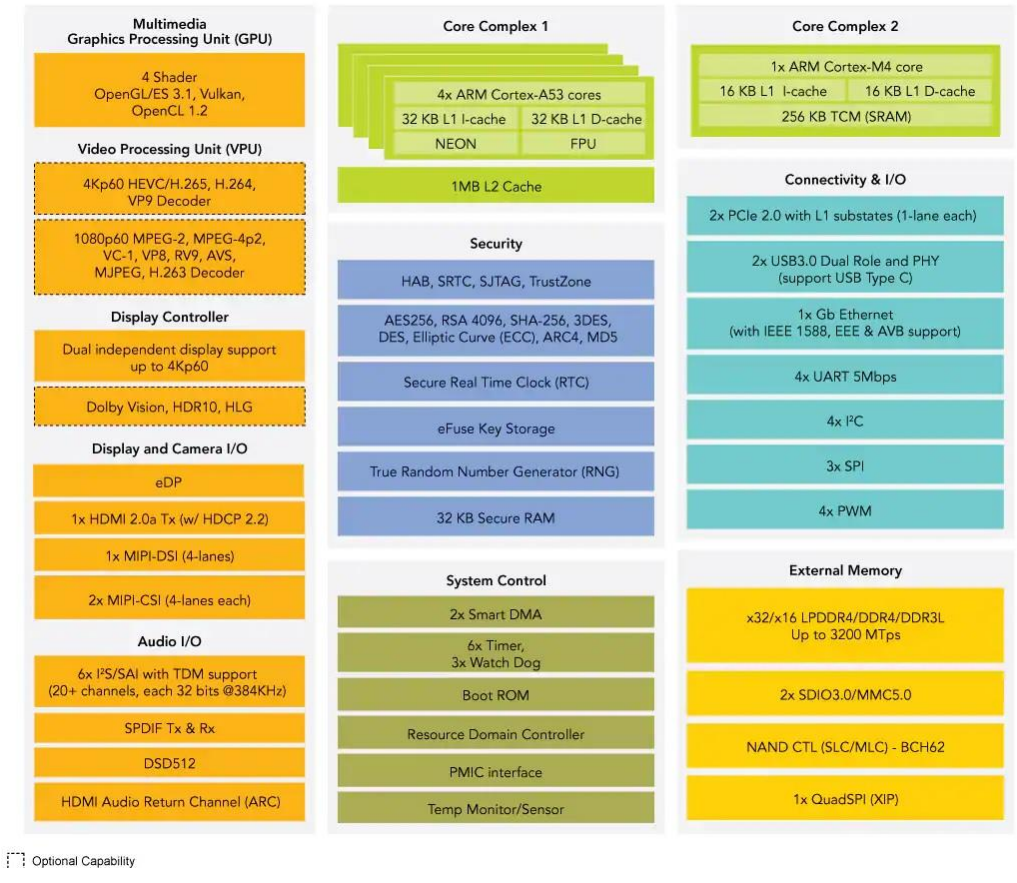

Figure 6 NXP iMX8M Processors Block Diagram

4 SMARC EXPANSION CONNECTOR INTERFACE

4.1 SMARC INTERFACE DEFINITION

IGEP™ SMARC iMX8M has a 314-pin SMARC interface (156 on TOP side and 158 on BOTTOM side), providing source power and 1V8 CMOS signals to support lots of iMX8M processor features which could be used in custom application. The module sizes are 82mm x 50mm as the SMARC standard defines. The module pins are numbered as P1 - P156 (TOP side) and S1 - S158 (BOTTOM side).

Next figure shows the area and pin numbering of the SMARC interface.

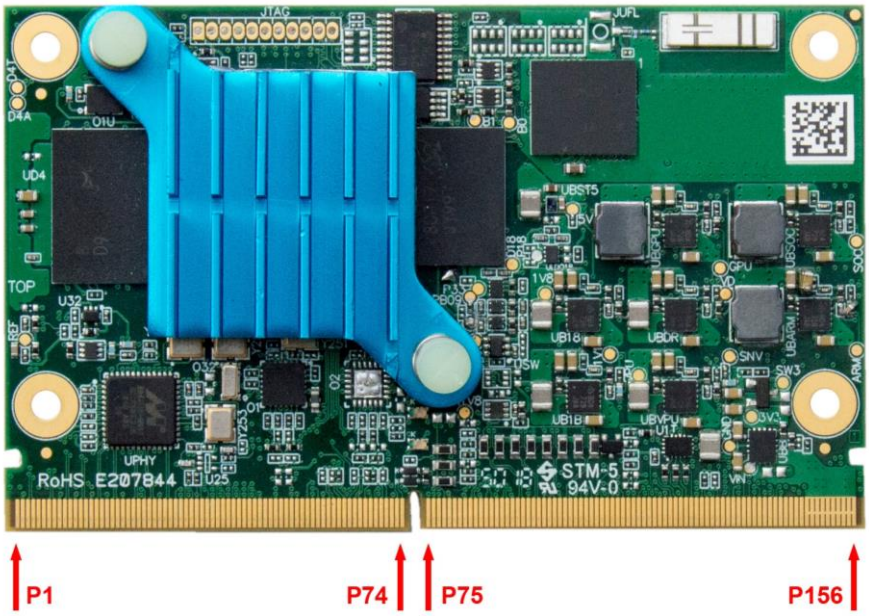

Figure 7 SMARC interface area (TOP Side)

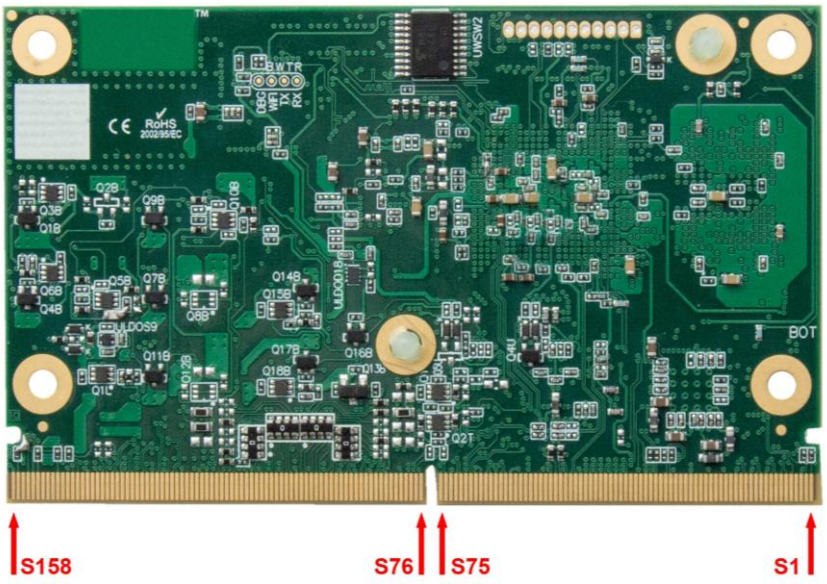

Figure 8 SMARC interface area (BOTTOM Side)

The IGEP™ SMARC iMX8M modules can be inserted like a target through this SMARC interface to any of the standard connectors existing on the market. Next table shows some valid references (consult the page 73 on the SMARC 2.1 Specification to find more information).

Manufacturer	Part Number	Height
FOXCONN	AS0B821-S43B-*H	4,3 mm
FOXCONN	AS0B821-S43N-*H	4,3 mm
FOXCONN	AS0B826-S43B-*H	4,3 mm
FOXCONN	AS0B826-S43N-*H	4,3 mm
JAE	MM70-314B2-1-R500	4,3 mm
Aces	91781-314 2 8-001	5,2 mm
FOXCONN	AS0B821-S55B-*H	5,50 mm
FOXCONN	AS0B821-S55N-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B821-S78B-*H	7,80 mm
FOXCONN	AS0B821-S78N-*H	7,80 mm
FOXCONN	AS0B826-S78B-*H	7,80 mm
FOXCONN	AS0B826-S78N-*H	7,80 mm
Yamaichi	CN113-314-2001	7,80 mm

Table 3 Valid SMARC connector part numbers

Developers must consider the SMARC connector height according to their expansion board needs.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards.

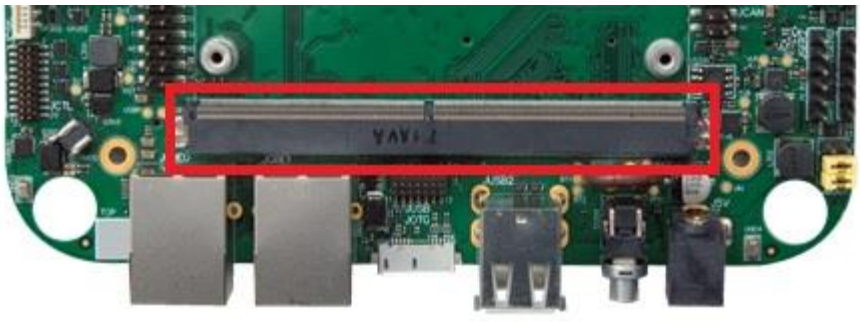

Figure 9 SMARC CONNECTOR

4.2 PINOUT TABLE OF SMARC (VERSION) EXPANSION INTERFACE

This chapter contains all the pinout details for the SMARC-314 expansion interface. The table below shows the meaning of each column in table 5, where is collected all the pins and its main functions.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC-314 interface. It is either for Primary Side (Top Side, P#) and Secondary Side (Bottom Side, S#)	
VOLTAGE LEVEL	Signal Level Voltage	
	5V	5 V signal
	3V3	3,3 V signal
	1V8	1,8 V signal
	DS	Differential analog signaling.
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface.
	LVDS D-PHY	LVDS signaling used for MIPI CSI camera interfaces.
	LVDS PCIe	LVDS signaling used for PCIe interfaces according to the PCI Express specification.
	TMDS HDMI	LVDS signaling used for HDMI display interfaces.
	USB	DC coupled differential signaling used for traditional (non-Super-Speed) USB signals
	USB SS	LVDS signaling used for Super Speed USB 3.0
	GND	Digital ground.
	RSV	Reserved.
	NC	No connected. This pin should be floating.
TYPE	Indicates pin type.	
	Power	Power signal.
	I CMOS	CMOS input pin.
	O CMOS	CMOS output pin.
	I/O CMOS	CMOS input and output pin.
	O OD CMOS	Open drain output pin.
	I/O OD CMOS	Open drain input and output pin.
	NC	No connected. This pin should be floating.
MAIN FUNCTION	Main or suggested function.	
COMMENTS	Clarification for the related SMARC-314 interface pin. See device chapter for more information.	

Table 4 SMARC expansion interface information

COLORS	INFORMATION
	Power Sources (Supply Voltages)
	Signal Level Voltage (Digital and Analog Ground)
	Control Signals
	Ethernet
	USB connections
	I2C
	SPI
	Wifi/Bluetooth and SD/SD card interface
	UART
	I2S
	CAN bus
	GPIOs
	Analog Inputs
	DVI
	LCD
	RTC Battery

Table 5 Colors Key

The following table includes all the pins and its description. Please, be careful with the name of pins related to Primary (Top side, pins PXXX) and Secondary (Bottom side, pins SXXX) sides of SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Primary (Top) Side				
P1	NC	NC	Not connected	Not connected
P2	GND	Power	GND	Digital ground
P3	LVDS D-PHY	I CMOS	CSI1_CK+	CSI1 differential Clock input.
P4	LVDS D-PHY	I CMOS	CSI1_CK-	CSI1 differential Clock input.
P5	NC	NC	Not connected	Not connected
P6	NC	NC	Not connected	Not connected
P7	LVDS D-PHY	I CMOS	CSI1_D0+	CSI1 D0 differential data input.
P8	LVDS D-PHY	I CMOS	CSI1_D0-	CSI1 D0 differential data input.
P9	GND	Power	GND	Digital ground
P10	LVDS D-PHY	I CMOS	CSI1_D1+	CSI1 D1 differential data input.
P11	LVDS D-PHY	I CMOS	CSI1_D1-	CSI1 D1 differential data input.
P12	GND	Power	GND	Digital ground
P13	LVDS D-PHY	I CMOS	CSI1_D2+	CSI1 D2 differential data input.
P14	LVDS D-PHY	I CMOS	CSI1_D2-	CSI1 D2 differential data input.
P15	GND	Power	GND	Digital ground
P16	LVDS D-PHY	I CMOS	CSI1_D3+	CSI1 D3 differential data input.
P17	LVDS D-PHY	I CMOS	CSI1_D3-	CSI1 D3 differential data input.
P18	GND	Power	GND	Digital ground
P19	GBE MDI	I/O CMOS	GBE0_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P20	GBE MDI	I/O CMOS	GBE0_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P21	3V3	O OD CMOS	GBE0_LINK100#	Link Speed Indication LED for GBE0 100Mbps
P22	3V3	O OD CMOS	GBE0_LINK1000#	Link Speed Indication LED for GBE0 1000Mbps.
P23	GBE MDI	I/O CMOS	GBE0_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P24	GBE MDI	I/O CMOS	GBE0_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).

P25	3V3	O OD CMOS	GBE0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity
P26	GBE MDI	I/O CMOS	GBE0_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P27	GBE MDI	I/O CMOS	GBE0_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P28	3V3	O CMOS	GBE0_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
P29	GBE MDI	I/O CMOS	GBE0_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P30	GBE MDI	I/O CMOS	GBE0_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P31	1V8	O CMOS	SPI0_CS1#	SPI0 Master Chip Select 1. Related to GPIO3_20 (iMX8M processor ball L5).
P32	GND	Power	GND	Digital ground
P33	3V3	I OD CMOS	SDIO_WP	SDIO card 4-bit Interface: Write Protect.
P34	3V3	I/O CMOS	SDIO_CMD	SDIO card 4-bit Interface: Command Line.
P35	3V3	I OD CMOS	SDIO_CD#	SDIO card 4-bit Interface: Card Detect.
P36	3V3	O CMOS	SDIO_CK	SDIO card 4-bit Interface: Clock. (1) (2)
P37	3V3	O CMOS	SDIO_PWR_EN	SDIO card 4-bit Interface: Card Power Enable.
P38	GND	Power	GND	Digital ground
P39	3V3	I/O CMOS	SDIO_D0	SDIO card 4-bit Interface: data path (D0).
P40	3V3	I/O CMOS	SDIO_D1	SDIO card 4-bit Interface: data path (D1).
P41	3V3	I/O CMOS	SDIO_D2	SDIO card 4-bit Interface: data path (D2).
P42	3V3	I/O CMOS	SDIO_D3	SDIO card 4-bit Interface: data path (D3).
P43	1V8	O CMOS	SPI0_CS0#	SPI0 Master Chip Select 0
P44	1V8	O CMOS	SPI0_CK	SPI0 Clock
P45	1V8	I CMOS	SPI0_DIN	SPI0 Master data input
P46	1V8	O CMOS	SPI0_DO	SPI0 Master data output
P47	GND	Power	GND	Digital ground
P48	NC	NC	Not connected	Not connected
P49	NC	NC	Not connected	Not connected
P50	GND	Power	GND	Digital ground

P51	NC	NC	Not connected	Not connected
P52	NC	NC	Not connected	Not connected
P53	GND	Power	GND	Digital ground
P54	1V8	O CMOS	SPI1_CS0#	SPI1 Master Chip Select 0 (1) (3)
P55	NC	NC	Not connected	Not connected
P56	1V8	O CMOS	SPI1_CK	SPI1 Clock (1) (3)
P57	1V8	I CMOS	SPI1_IO_0	SPI1 Master data input (1) (3)
P58	1V8	O CMOS	SPI1_IO_1	SPI1 Master data output (1) (3)
P59	GND	Power	GND	Digital ground
P60	USB	I/O CMOS	USB0+	UBS1: USB2.0 differential data input.
P61	USB	I/O CMOS	USB0-	UBS1: USB2.0 differential data input.
P62	3V3	I/O OD CMOS	USB0_EN_OC#	USB1: USB2.0 enable pin. Active low. Related to GPIO1_13 (iMX8M processor ball K6).
P63	5V	I CMOS	USB0_VBUS_DET	USB1: USB2.0 Host power detection when this port is used as a device.
P64	3V3	I CMOS	USB0_OTG_ID	USB1: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port.
P65	USB	I/O CMOS	USB1+	UBS2: USB2.0 differential data input.
P66	USB	I/O CMOS	USB1-	UBS2: USB2.0 differential data input.
P67	3V3	I/O OD CMOS	USB1_EN_OC#	USB2: USB2.0 enable pin. Active low. Related to GPIO1_15 (iMX8M processor ball J6).
P68	GND	Power	GND	Digital ground
P69	NC	NC	Not connected	Not connected
P70	NC	NC	Not connected	Not connected
P71	NC	NC	Not connected	Not connected
P72	NC	NC	Not connected	Not connected
P73	3V3	I CMOS	PCIE_B_PRSNT#	PCIeB: Hotplug presence detect. Active low. Related to GPIO1_3 (iMX8M processor ball P4).
P74	3V3	I CMOS	PCIE_A_PRSNT#	PCIeA: Hotplug presence detect. Active low. Related to GPIO1_3 (iMX8M processor ball P4).
P75	3V3	I CMOS	PCIE_A_RST#	PCIeA: Port reset output. Active low. Related to GPIO1_10 (iMX8M processor ball M7).
P76	NC	NC	Not connected	Not connected

P77	3V3	IO OD CMOS	PCIE_B_CKREQ#	PCIe Port B clock request. Associated with GPIO5_21 (iMX8M processor ball F9).
P78	3V3	O OD CMOS	PCIE_A_CKREQ#	PCIe Port A clock request. Associated with GPIO5_20 (iMX8M processor ball F8).
P79	GND	Power	GND	Digital ground
P80	NC	NC	Not connected	Not connected
P81	NC	NC	Not connected	Not connected
P82	GND	Power	GND	Digital ground
P83	LVDS PCIe	O CMOS	PCIE_A_REFCK+	PCIeA: Differential PCIe Link reference clock output DC coupled.
P84	LVDS PCIe	O CMOS	PCIE_A_REFCK-	PCIeA: Differential PCIe Link reference clock output DC coupled.
P85	GND	Power	GND	Digital ground
P86	LVDS PCIe	I CMOS	PCIE_A_RX+	PCIeA: Differential PCIe Link receive data pair 0
P87	LVDS PCIe	I CMOS	PCIE_A_RX-	PCIeA: Differential PCIe Link receive data pair 0
P88	GND	Power	GND	Digital ground
P89	LVDS PCIe	O CMOS	PCIE_A_TX+	PCIeA: Differential PCIe Link transmit data pair 0
P90	LVDS PCIe	O CMOS	PCIE_A_TX-	PCIeA: Differential PCIe Link transmit data pair 0
P91	GND	Power	GND	Digital ground
P92	TMDS HDMI	O CMOS	HDMI_D2+	HDMI differential data input D2.
P93	TMDS HDMI	O CMOS	HDMI_D2-	HDMI differential data input D2.
P94	GND	Power	GND	Digital ground
P95	TMDS HDMI	O CMOS	HDMI_D1+	HDMI differential data input D1.
P96	TMDS HDMI	O CMOS	HDMI_D1-	HDMI differential data input D1.
P97	GND	Power	GND	Digital ground
P98	TMDS HDMI	O CMOS	HDMI_D0+	HDMI differential data input D0.
P99	TMDS HDMI	O CMOS	HDMI_D0-	HDMI differential data input D0.
P100	GND	Power	GND	Digital ground
P101	TMDS HDMI	O CMOS	HDMI_CK+	HDMI differential clock output pair. Clock lines
P102	TMDS HDMI	O CMOS	HDMI_CK-	HDMI differential clock output pair. Clock Lines

P103	GND	Power	GND	Digital ground
P104	1V8	I CMOS	HDMI_HPD	HDMI Hot Plug detect input.
P105	1V8	I/O OD CMOS	HDMI_CTRL_CK	I2C Clock line dedicated to HDMI.
P106	1V8	I/O OD CMOS	HDMI_CTRL_DAT	I2C Data line dedicated to HDMI.
P107	1V8	I/O CMOS	HDMI_CEC	CEC Consumer Electronic Control.
P108	1V8	I/O CMOS	GPIO0/CAM0_PWR#	SMARC GPIO pin. Related to GPIO3_0 (iMX8M processor ball G19).
P109	1V8	I/O CMOS	GPIO1/CAM1_PWR#	SMARC GPIO pin. Related to GPIO3_1 (iMX8M processor ball H19).
P110	1V8	I/O CMOS	GPIO2CAM0_RST#	SMARC GPIO pin. Related to GPIO3_2 (iMX8M processor ball G21).
P111	1V8	I/O CMOS	GPIO3/CAM1_RST#	SMARC GPIO pin. Related to GPIO3_3 (iMX8M processor ball F21).
P112	1V8	I/O CMOS	GPIO4/HDA_RST#	SMARC GPIO pin. Related to GPIO3_4 (iMX8M processor ball H20).
P113	1V8	I/O CMOS	GPIO5/PWM_OUT	SMARC GPIO pin / PWM3. Related to GPIO5_3 (iMX8M processor ball F6).
P114	1V8	I/O CMOS	GPIO6/TACHIN	SMARC GPIO pin. Related to GPIO3_5 (iMX8M processor ball H21).
P115	1V8	I/O CMOS	GPIO7/PCAM_FLD	SMARC GPIO pin. Related to GPIO3_14 (iMX8M processor ball M20).
P116	1V8	I/O CMOS	GPIO8/CAN0_ERR#	SMARC GPIO pin. Related to GPIO3_15 (iMX8M processor ball K19).
P117	1V8	I/O CMOS	GPIO9/CAN1_ERR#	SMARC GPIO pin. Related to GPIO3_16 (iMX8M processor ball K20).
P118	1V8	I/O CMOS	GPIO10	SMARC GPIO pin. Related to GPIO3_17 (iMX8M processor ball K22).
P119	1V8	I/O CMOS	GPI11	SMARC GPIO pin. Related to GPIO3_18 (iMX8M processor ball K21).
P120	GND	Power	GND	Digital ground
P121	1V8	I/O OD CMOS	I2C_PM_CK	Power management I2C bus CLK
P122	1V8	I/O OD CMOS	I2C_PM_DAT	Power management I2C bus DATA
P123	1V8	I OD CMOS	BOOT_SEL0#	Input straps determine the Module boot device. Active low.
P124	1V8	I OD CMOS	BOOT_SEL1#	Input straps determine the Module boot device. Active low.
P125	1V8	I OD CMOS	BOOT_SEL2#	Input straps determine the Module boot device. Active low.

P126	1V8	O CMOS	RESET_OUT#	General purpose reset output to Carrier board. Active low. Related to GPIO3_11 (iMX8M processor ball J22).
P127	1V8	I OD CMOS	RESET_IN#	Reset input from Carrier board. Active low.
P128	1V8	I OD CMOS	POWER_BTN#	Power button input from carrier board. Active low. Related to GPIO3_12 (iMX8M processor ball L19).
P129	1V8	O CMOS	SER0_TX	UART1: Asynchronous serial port 1 data out. (4)
P130	1V8	I CMOS	SER0_RX	UART1: Asynchronous serial port 1 data in. (5)
P131	1V8	O CMOS	SER0_RTS#	UART1: Request to Send handshake line. Active low.
P132	1V8	I CMOS	SER0_CTS#	UART1: Clear to Send handshake line. Active low.
P133	GND	Power	GND	Digital ground
P134	1V8	O CMOS	SER1_TX	UART2: Asynchronous serial port 1 data out.
P135	1V8	I CMOS	SER1_RX	UART2: Asynchronous serial port 1 data in.
P136	1V8	O CMOS	SER2_TX	UART3: Asynchronous serial port 1 data out. (1) (6)
P137	1V8	I CMOS	SER2_RX	UART3: Asynchronous serial port 1 data in. (1) (6)
P138	1V8	O CMOS	SER2_RTS#	UART3: Request to Send handshake line. Active low. (1) (6)
P139	1V8	I CMOS	SER2_CTS#	UART3: Clear to Send handshake line. Active low. (1) (6)
P140	1V8	O CMOS	SER3_TX	UART4: Asynchronous serial port 1 data out.
P141	1V8	I CMOS	SER3_RX	UART4: Asynchronous serial port 1 data in.
P142	GND	Power	GND	Digital ground
P143	NC	NC	Not connected	Not connected
P144	NC	NC	Not connected	Not connected
P145	NC	NC	Not connected	Not connected
P146	NC	NC	Not connected	Not connected
P147	5V	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 3V to 5V25
P148	5V	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V to 5V25

P149	5V	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 3V to 5V25
P150	5V	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 3V to 5V25
P151	5V	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 3V to 5V25
P152	5V	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 3V to 5V25
P153	5V	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 3V to 5V25
P154	5V	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 3V to 5V25
P155	5V	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 3V to 5V25
P156	5V	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 3V to 5V25
Secondary (Bottom) Side				
S1	1V8	IO OD CMOS	I2C_CAM1_CK	I2C4: Clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S2	1V8	IO OD CMOS	I2C_CAM1_DATA	I2C 4: Data signal. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S3	GND	Power	GND	Digital ground
S4	RSV	RSV	Reserved	Reserved
S5	1V8	IO OD CMOS	I2C_CAM0_CK	I2C 3: Clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S6	1V8	O CMOS	CAM_MCK	Master clock for CSI camera support (may be used for CSI1 and CSI2).
S7	1V8	IO OD CMOS	I2C_CAM0_DAT	I2C 3: Data signal. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S8	LVDS D-PHY	I CMOS	CSI0_CK+	CSI2 differential Clock input.
S9	LVDS D-PHY	I CMOS	CSI0_CK-	CSI2 differential Clock input.
S10	GND	Power	GND	Digital ground
S11	LVDS D-PHY	I CMOS	CSI0_D0+	CSI2 D0 differential data input.
S12	LVDS D-PHY	I CMOS	CSI0_D0-	CSI2 D0 differential data input.
S13	GND	Power	GND	Digital ground
S14	LVDS D-PHY	I CMOS	CSI0_D1+	CSI2 D1 differential data input.
S15	LVDS D-PHY	I CMOS	CSI0_D1-	CSI2 D1 differential data input.

S16	GND	Power	GND	Digital ground
S17	GBE MDI	I/O CMOS	GBE1_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S18	GBE MDI	I/O CMOS	GBE1_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S19	3V3	O CMOS	GBE1_LINK100#	Link Speed indication LED for GBE1 1000 Mbps.
S20	GBE MDI	I/O CMOS	GBE1_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S21	GBE MDI	I/O CMOS	GBE1_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S22	3V3	O CMOS	GBE1_LINK1000#	Link Speed indication LED for GBE1 1000 Mbps.
S23	GBE MDI	I/O CMOS	GBE1_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S24	GBE MDI	I/O CMOS	GBE1_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S25	GND	Power	GND	Digital ground
S26	GBE MDI	I/O CMOS	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S27	GBE MDI	I/O CMOS	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S28	3V3	O CMOS	GBE1_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
S29	LVDS D-PHY	I CMOS	CSI2_D2+	CSI1 D2 differential data input.
S30	LVDS D-PHY	I CMOS	CSI2_D2-	CSI1 D2 differential data input.
S31	3V3	O OD CMOS	GBE1_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity
S32	LVDS D-PHY	I CMOS	CSI2_D3+	CSI1 D3 differential data input.
S33	LVDS D-PHY	ICMOS	CSI2_D3-	CSI1 D3 differential data input.
S34	GND	Power	GND	Digital ground
S35	NC	NC	Not connected	Not connected
S36	NC	NC	Not connected	Not connected
S37	5V	I CMOS	USB3_VBUS_DET	USB3: USB2.0 Host power detection when this port is used as a device.
S38	1V8	O CMOS	AUDIO_MCK	SAI2: Master Clock output to Audio codecs.

S39	1V8	I/O CMOS	I2S0_LRCK	SAI2: Left & Right Audio synchronization clock.
S40	1V8	O CMOS	I2S0_SDOUT	SAI2: Digital Audio output.
S41	1V8	I CMOS	I2S0_SDIN	SAI2: Digital Audio input.
S42	1V8	I/O CMOS	I2S0_CK	SAI2: Digital Audio clock.
S43	1V8	I/O CMOS	I2S1_LRCK	SAI3: Left & Right Audio synchronization clock. (1)
S44	1V8	O CMOS	I2S1_SDOUT	SAI3: Digital Audio output. (1)
S45	1V8	I CMOS	I2S1_SDIN	SAI3: Digital Audio input. (1)
S46	1V8	I/O CMOS	I2S1_CK	SAI3: Digital Audio clock. (1)
S47	GND	Power	GND	Digital ground
S48	1V8	I/O OD CMOS	I2C_GP_CK	I2C1: Clock signal.
S49	1V8	I/O OD CMOS	I2C_GP_DAT	I2C1: Data signal.
S50	1V8	I/O CMOS	I2S2_LRCK	SAI1: Left & Right Audio synchronization clock.
S51	1V8	O CMOS	I2S2_SDOUT	SAI1: Digital Audio output.
S52	1V8	I CMOS	I2S2_SDIN	SAI1: Digital Audio input.
S53	1V8	I/O CMOS	I2S2_CK	SAI1: Digital Audio clock.
S54	NC	NC	Not connected	Not connected
S55	NC	NC	Not connected	Not connected
S56	NC	NC	Not connected	Not connected
S57	NC	NC	Not connected	Not connected
S58	NC	NC	Not connected	Not connected
S59	NC	NC	Not connected	Not connected
S60	NC	NC	Not connected	Not connected
S61	GND	Power	GND	Digital ground
S62	USB SS	O CMOS	USB3_SSTX+	USB1 SS: TX differential pair.
S63	USB SS	O CMOS	USB3_SSTX-	USB1 SS: TX differential pair.
S64	GND	Power	GND	Digital ground
S65	USB SS	I CMOS	USB3_SSRX+	USB1 SS: RX differential pair.
S66	USB SS	I CMOS	USB3_SSRX-	USB1 SS: RX differential pair.
S67	GND	Power	GND	Digital ground
S68	NC	NC	Not connected	Not connected

S69	NC	NC	Not connected	Not connected
S70	GND	Power	GND	Digital ground
S71	USB SS	O CMOS	USB2_SSTX+	USB2 SS: TX differential pair.
S72	USB SS	O CMOS	USB2_SSTX-	USB2 SS: TX differential pair.
S73	GND	Power	GND	Digital ground
S74	USB SS	I CMOS	USB2_SSRX+	USB2 SS: RX differential pair.
S75	USB SS	I CMOS	USB2_SSRX-	USB2 SS: RX differential pair.
S76	3V3	O CMOS	PCIE_B_RST#	PCIeB: Port reset output. Active low. Related to GPIO1_3
S77	NC	NC	Not connected	Not connected
S78	NC	NC	Not connected	Not connected
S79	NC	NC	Not connected	Not connected
S80	GND	Power	GND	Digital ground
S81	NC	NC	Not connected	Not connected
S82	NC	NC	Not connected	Not connected
S83	GND	Power	GND	Digital ground
S84	LVDS PCIe	O CMOS	PCIE_B_REFCK+	PCIeB: Differential PCIe Link reference clock output DC coupled.
S85	LVDS PCIe	O CMOS	PCIE_B_REFCK-	PCIeB: Differential PCIe Link reference clock output DC coupled.
S86	GND	Power	GND	Digital ground
S87	LVDS PCIe	I CMOS	PCIE_B_RX+	PCIeB: Differential PCIe Link receive data pair 0
S88	LVDS PCIe	I CMOS	PCIE_B_RX-	PCIeB: Differential PCIe Link receive data pair 0
S89	GND	Power	GND	Digital ground
S90	LVDS PCIe	O CMOS	PCIE_B_TX+	PCIeB: Differential PCIe Link transmit data pair 0
S91	LVDS PCIe	O CMOS	PCIE_B_TX-	PCIeB: Differential PCIe Link transmit data pair 0
S92	GND	Power	GND	Digital ground
S93	1V8	O CMOS	DP0_ LANE 0+	SAI1: Primary DP Port Differential
S94	1V8	O CMOS	DP0_ LANE 0-	SAI1: Primary DP Port Differential
S95	1V8	I CMOS	DP0_SEL	SAI1: DP Selection

S96	1V8	O CMOS	DP0_ LANE 1+	SAI1: Primary DP Port Differential.
S97	1V8	O CMOS	DP0_ LANE 1-	SAI1: Primary DP Port Differential.
S98	1V8	I CMOS	DP0_HDP	SAI1: DP Hot Plug detect input.
S99	1V8	O CMOS	DP0_ LANE 2+	SAI1: Primary DP Port Differential.
S100	1V8	O CMOS	DP0_ LANE 2-	SAI1: Primary DP Port Differential.
S101	GND	Power	GND	Digital ground
S102	1V8	O CMOS	DP0_ LANE 3+	SAI1: Primary DP Port Differential.
S103	1V8	O CMOS	DP0_ LANE 3-	SAI1: Primary DP Port Differential.
S104	3V3	I CMOS	USB3_OTG_ID/SAI1_RXD3	SAI1: Primary DP Port Differential /USB2.0 OTG ID input.
S105	3V3	I/ O CMOS	DP0_X+	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control
S106	3V3	I/ O CMOS	DP0_X-	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control
S107	1V8	O CMOS	LCD1_BKLT_EN	SAI1: Secondary Panel Backlight Enable
S108	DS	O CMOS	LVDS1-eDSI1-DSII_CK+	SAI1: Secondary LVDS Channel Differential Pair Clock Lines
S109	DS	O CMOS	LVDS1-eDSI1-DSII_CK-	SAI1: Secondary LVDS Channel Differential Pair Clock Lines
S110	GND	Power	GND	Digital ground
S111	DS	O CMOS	LVDS1-eDSI1-DSII_0-	SAI1: Secondary LVDS Channel Differential Pair Data Lines
S112	NC	NC	Not connected	Not connected
S113	NC	NC	Not connected	Not connected
S114	NC	NC	Not connected	Not connected
S115	NC	NC	Not connected	Not connected
S116	NC	NC	Not connected	Not connected
S117	NC	NC	Not connected	Not connected
S118	NC	NC	Not connected	Not connected
S119	GND	Power	GND	Digital ground
S120	NC	NC	Not connected	Not connected
S121	NC	NC	Not connected	Not connected
S122	NC	NC	Not connected	Not connected

S123	NC	NC	Not connected	Not connected
S124	GND	Power	GND	Digital ground
S125	DS	O CMOS	DSI0_D0+	DSI: Data pair 0.
S126	DS	O CMOS	DSI0_D0-	DSI: Data pair 0.
S127	1V8	O CMOS	LCD0_BKLT_EN	SAI3: LCD Primary Panel Backlight Enable.
S128	DS	O CMOS	DSI0_D1+	DSI: Data pair 1.
S129	DS	O CMOS	DSI0_D1-	DSI: Data pair 1.
S130	GND	Power	GND	Digital ground
S131	DS	O CMOS	DSI0_D2+	DSI: Data pair 2.
S132	DS	O CMOS	DSI0_D2-	DSI: Data pair 2.
S133	1V8	O CMOS	LCD0_VDD_EN/ GPIO 9	SMARC GPIO pin. Related to GPIO3_9 (iMX8M processor ball J21)
S134	1V8	I/O CMOS	DSI0_CLK+	DSI: Clock pair.
S135	1V8	I/O CMOS	DSI0_CLK-	DSI: Clock pair.
S136	GND	Power	GND	Digital ground
S137	DS	O CMOS	DSI0_D3+	DSI: Data pair 3.
S138	DS	O CMOS	DSI0_D3-	DSI: Data pair 3.
S139	1V8	I/O CMOS	I2C_LCD_CK	I2C4 Clock to Read LCD Display EDID EEPROMs
S140	1V8	I/O CMOS	I2C_LCD_DAT	I2C4 Data to Read LCD Display EDID EEPROMs
S141	1V8	O CMOS	LCD0_BKLT_PWM	SAI3: LCD Primary Panel Brightness Contro. Related to GPIO5_2(iMX8M processor ball D3)
S142	NC	NC	Not connected	Not connected
S143	GND	Power	GND	Digital ground
S144	NC	NC	Not connected	Not connected
S145	1V8	O CMOS	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active.
S146	3V3	I OD CMOS	PCIE_WAKE	PCIe wake up interrupt to host. Common to PCIe links A, B, C, D. Related to GPIO1_7 (iMX8M processor ball N6).
S147	3V	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.
S148	NC	NC	Not connected	Not connected

S149	1V8	I OD CMOS	SLEEP#	Sleep indicator from Carrier Board. Related to GPIO3_6 (iMX8M processor ball G20).
S150	NC	NC	Not connected	Not connected
S151	NC	NC	Not connected	Not connected
S152	NC	NC	Not connected	Not connected
S153	1V8	O CMOS	CARRIER_STBY#	Standby state. Related to GPIO3_7 (iMX8M processor ball J20).
S154	1V8	O CMOS	CARRIER_PWR_ON#	Signal to enable Carrier Board power on. Related to GPIO3_8 (iMX8M processor ball H22).
S155	1V8	I OD CMOS	FORCE_RECOV#	Force Recovery
S156	NC	NC	Not connected	Not connected
S157	1V8	I OD CMOS	TEST#	Test. Related to GPIO3_10 (iMX8M processor ball L20).
S158	GND	Power	GND	Digital ground

Notes

(1)	This function is only present in No WiFi models (some pins are shared with WiFi SDIO).
(2)	In WiFi models these pins are only available during Boot process.
(3)	This function is shared with UART3.
(4)	It is also connected to TX in JTAG connector.
(5)	It is also connected to RX in JTAG connector.
(6)	These pins are shared with SPI1.

Table 6 SMARC pinout description

5 PRODUCT SPECIFICATIONSUMMARY

5.1 POWER SOURCES

5.1.1 Supply Voltage

SMARC iMX8M module cannot be used as stand-alone module, so keep in mind that expansion board must power VIN signal input. This signal is defined into SMARC interface and can be in a range between 3V to 5V25. For more information see electrical characteristics table in Chapter 7 ELECTRICAL CHARACTERISTICS.

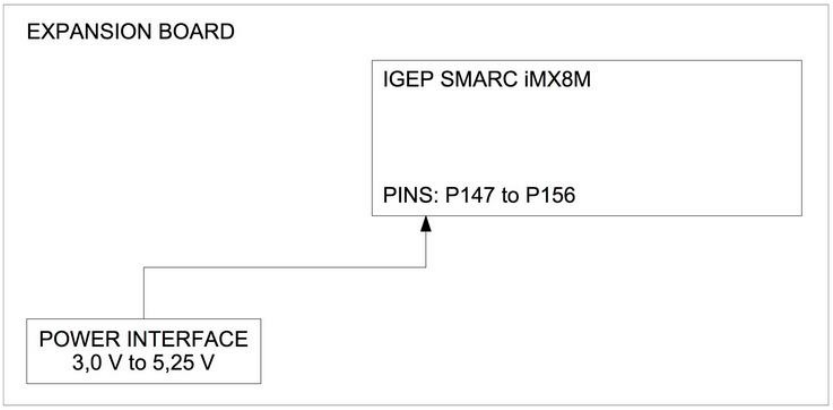

Figure 10 Power Supply Input Diagram

In the following table there is a summary of all Power Supply pins available related to the MXM3 SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
5V Input Power				
P147	5V	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 3V to 5V25
P148	5V	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 3V to 5V25
P149	5V	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 3V to 5V25
P150	5V	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 3V to 5V25
P151	5V	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 3V to 5V25
P152	5V	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 3V to 5V25
P153	5V	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 3V to 5V25
P154	5V	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 3V to 5V25
P155	5V	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 3V to 5V25
P156	5V	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 3V to 5V25

Table 7 Power Supply pins

5.1.2 Digital Ground

All the digital GND pins are internally connected. However, the user has to considerer how many of them should connect according to the total consumption of the complete circuit (SMARC iMX8M and the developed base board). At the same time, to make easier the buses routing, the GND connection chosen should be the nearest to the function used.

It shall be a minimum of 4 GND pins connected, distributed in the most possible equal way along the MXM3 SMARC connector, to get an equalized ground.

In the following table there is a summary of all GND pins available related to the MXM3 SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Digital Ground				
P2	GND	Power	GND	Digital ground
P9	GND	Power	GND	Digital ground
P12	GND	Power	GND	Digital ground
P15	GND	Power	GND	Digital ground
P18	GND	Power	GND	Digital ground
P32	GND	Power	GND	Digital ground
P38	GND	Power	GND	Digital ground
P47	GND	Power	GND	Digital ground
P50	GND	Power	GND	Digital ground
P53	GND	Power	GND	Digital ground
P59	GND	Power	GND	Digital ground
P68	GND	Power	GND	Digital ground
P79	GND	Power	GND	Digital ground
P82	GND	Power	GND	Digital ground
P85	GND	Power	GND	Digital ground
P88	GND	Power	GND	Digital ground
P91	GND	Power	GND	Digital ground
P94	GND	Power	GND	Digital ground
P97	GND	Power	GND	Digital ground
P100	GND	Power	GND	Digital ground
P103	GND	Power	GND	Digital ground
P120	GND	Power	GND	Digital ground

P133	GND	Power	GND	Digital ground
P142	GND	Power	GND	Digital ground
S3	GND	Power	GND	Digital ground
S10	GND	Power	GND	Digital ground
S13	GND	Power	GND	Digital ground
S16	GND	Power	GND	Digital ground
S25	GND	Power	GND	Digital ground
S34	GND	Power	GND	Digital ground
S47	GND	Power	GND	Digital ground
S61	GND	Power	GND	Digital ground
S64	GND	Power	GND	Digital ground
S67	GND	Power	GND	Digital ground
S70	GND	Power	GND	Digital ground
S73	GND	Power	GND	Digital ground
S80	GND	Power	GND	Digital ground
S83	GND	Power	GND	Digital ground
S86	GND	Power	GND	Digital ground
S89	GND	Power	GND	Digital ground
S92	GND	Power	GND	Digital ground
S101	GND	Power	GND	Digital ground
S110	GND	Power	GND	Digital ground
S119	GND	Power	GND	Digital ground
S124	GND	Power	GND	Digital ground
S130	GND	Power	GND	Digital ground
S136	GND	Power	GND	Digital ground
S143	GND	Power	GND	Digital ground
S158	GND	Power	GND	Digital ground

Table 8 Digital Ground pins

5.2 CONTROL SIGNALS

There are different pins used as general control signals. They are related to Boot Mode, Reset functions, the use of an External Pushbutton and some pins related with the Module State Pins.

5.2.1 Boot Modes

There are three pins in the MXM3 SMARC connector which can be used to fix the boot mode of the module (pins 123 to 125 on Top side). They are active low. With them is possible to fix from which device will boot up the module. Next table offers all possible ways.

BOOT2 (P125)	BOOT1 (P124)	BOOT0 (P123)	BOOT MODE
0	0	0	RESERVED
0	0	1	Carrier SD Card
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	RESERVED
1	0	1	Remote boot (Network (GBE) or Serial)
1	1	0	Module eMMC Flash
1	1	1	RESERVED

Table 9 Boot Mode pins

Reserved positions are combinations which are not implemented in current SMARC module. Users must avoid using them since it would not be possible to complete a module boot up.

Please, be careful that **default position is '111'**. This is a reserved position and it is not possible to perform a complete module boot up since there is not an implemented Flash-SPI at Boot instructions. The User must use any of available combinations. In example, it is possible to boot from a SD-Card using combination '001'.

It is recommended to use a jumper header or a switch in series with a low resistor value (as a short circuit protector element) tied to GND in Carrier Board to control the values of these pins.

5.2.2 Reset pins

There are also two different Reset-IO possibilities. The first one is a General Reset RESET_OUT# (P126) and the other one is a RESET_IN# (P127).

Pin RESET_OUT# (P126) is general purpose reset output to Carrier Board. Related to GPIO3_11 (iMX8M processor ball J22).

Pin RESET_IN# (P127) is a Reset input from Carrier Board. In this case, when it is low state, Carrier forces a Module Reset.

5.2.3 External Pushbutton

Pin POWER_BTN# (P128) is to be used as Power-button input from Carrier Board. This is active low. Related to GPIO3_12 (iMX8M processor ball L19).

5.2.4 Module State Pins

- **Watchdog Timer output**

Pin WDT_TIME_OUT# (S145) Watchdog interrupt output. This is active low.

- **Sleep**

Pin SLEEP# (S149) - Carrier drives to float the line in in-activate state. Active low, level sensitive. Pulled up on Module. Driven by OD part on Carrier. Related to GPIO3_6 (iMX8M processor ball G20).

- **Carrier Standby**

Pin CARRIER_STBY# (S153) - Signal is Low when system is in a standby power state. Related to GPIO3_7 (iMX8M processor ball J20).

- **Carrier Power On**

Pin CARRIER_PWR_ON# (S154) - Carrier board circuits (apart from power management and power path circuits) should not be powered until the Module asserts this signal. Related to GPIO3_8 (iMX8M processor ball H22).

- **Force Recovery**

Pin FORCE_RECOV# (S155) - Low on this pin allows non-protected segments of Module boot device to be rewritten/restored from an external USB Host on Module USB0.

- **Test**

Pin TEST# (S157) - Held low by Carrier to invoke Module test functions. Pulled up on Module. Driven by OD part on Carrier. Related to GPIO3_10 (iMX8M processor ball L20).

The table below shows a summary of all control signals:

Pin	Volt Level	Type	Main Function	Comments
Boot Modes				
P123	1V8	I OD CMOS	BOOT_SEL0#	Input straps determine the Module boot device. Active low.
P124	1V8	I OD CMOS	BOOT_SEL1#	Input straps determine the Module boot device. Active low.
P125	1V8	I OD CMOS	BOOT_SEL2#	Input straps determine the Module boot device. Active low.
Reset functions				
P126	1V8	O CMOS	RESET_OUT#	General purpose reset output to Carrier board. Active low. Related to GPIO3_11 (iMX8M processor ball J22).
P127	1V8	I OD CMOS	RESET_IN#	Reset input from Carrier board. Active low.
External pushbutton				
P128	1V8	I OD CMOS	POWER_BTN#	Power button input from carrier board. Active low. Related to GPIO3_12 (iMX8M processor ball L19).

State pins				
S145	1V8	O CMOS	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active.
S149	1V8	I OD CMOS	SLEEP#	Sleep indicator from Carrier Board. Related to GPIO3_6 (iMX8M processor ball G20).
S153	1V8	O CMOS	CARRIER_STBY#	Standby state. Related to GPIO3_7 (iMX8M processor ball J20).
S154	1V8	O CMOS	CARRIER_PWR_ON#	Signal to enable Carrier Board power on. Related to GPIO3_8 (iMX8M processor ball H22).
S155	1V8	I OD CMOS	FORCE_RECOV#	Force Recovery
S157	1V8	I OD CMOS	TEST#	Test. Related to GPIO3_10 (iMX8M processor ball L20).

Table 10 Control Signals pins

5.3 ETHERNET

There are two available Gigabit Ethernet port in the module (10/100/1000 Mbps). Both ports come from a 3-Port Gigabit Ethernet Switch, whose third port is directly connected to iMX8M processor using a RGMII interface. The Switch used is a 3-Port Gigabit Ethernet Switch from Microchip (KSZ9893RNX).

A I2C bus (named I2C1 in the processor) can be used to configure the switch.

The module implements respective physical layers for each interface and a block of pins of SMARC-314 interface that can be connected directly to the Ethernet connectors. Both transmission and reception lines (TX and RX) are differential (there are a total of four pairs for etch Ethernet, and in the pin functions is indicated the Negative and Positive) and they should be connected to magnetics for isolation. The data lines must be equal length and symmetric and respect a 100 Ω differential impedance in the layout traces. The differential pairs must be isolated.

Moreover, the magnetics module has a critical effect, so it must be designed carefully. In order to obtain a smaller size, it is usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they must respect a separation under of 25 mm between them and the RJ45 connector, and 20 mm or greater between them and the SMARC-314 connector.

There is also possible to connect two LEDs. They are used to indicate the good functioning of the Ethernet connection. The first one (GBE0_LINK_ACT# and GBE1_LINK_ACT#) indicates the line activity (LED on indicates a valid link; LED blinking when there is data traffic). The second one (GBE0_LINK100# and GBE1_LINK100#)) is a link speed indication for 100 Mbps. These are usually in green and yellow color.

The last used pins are GBE0_CTREF and GBE1_CTREF. There are to be used as reference voltage for Carrier Board Ethernet magnetic (if it is required by the module GBE PHY).

The following table presents all the Ethernet 10/100/1000 Mbps pins:

Pin	Volt Level	Type	Main Function	Comments
P19	GBE MDI	I/O CMOS	GBE0_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P20	GBE MDI	I/O CMOS	GBE0_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
P21	3V3	O OD CMOS	GBE0_LINK100#	Link Speed Indication LED for GBE0 100 Mbps
P22	3V3	O OD CMOS	GBE0_LINK1000#	Link Speed Indication LED for GBE0 1000 Mbps.
P23	GBE MDI	I/O CMOS	GBE0_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P24	GBE MDI	I/O CMOS	GBE0_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
P25	3V3	O OD CMOS	GBE0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity
P26	GBE MDI	I/O CMOS	GBE0_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P27	GBE MDI	I/O CMOS	GBE0_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
P28	3V3	O CMOS	GBE0_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
P29	GBE MDI	I/O CMOS	GBE0_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
P30	GBE MDI	I/O CMOS	GBE0_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S17	GBE MDI	I/O CMOS	GBE1_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S18	GBE MDI	I/O CMOS	GBE1_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S19	3V3	O CMOS	GBE1_LINK100#	Link Speed indication LED for GBE1 100 Mbps.
S20	GBE MDI	I/O CMOS	GBE1_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S21	GBE MDI	I/O CMOS	GBE1_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S22	3V3	O CMOS	GBE1_LINK1000#	Link Speed indication LED for GBE1 1000 Mbps.
S23	GBE MDI	I/O CMOS	GBE1_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).

S24	GBE MDI	I/O CMOS	GBE1_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S26	GBE MDI	I/O CMOS	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S27	GBE MDI	I/O CMOS	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S28	3V3	O CMOS	GBE1_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)
S31	3V3	O OD CMOS	GBE1_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity

Table 11 Ethernet 10/100/1000 Mbps pins

For **Ethernet implementation examples**, you could consult the SMARC Design Guide 2.0 (page 72).

5.4 USB CONNECTIONS

There are available two USB 3.0 connections in the module. Because mandatory interfaces in SMARC are USB1 and USB2, these are configured as OTG (On-The-Go) and Host respectively. For this same reason, and to obtain a complete USB 3.0 interface with obligatory sets, there has been used different sets for each one.

- **USB 3.0 OTG**

The USB 3.0 OTG connection allows the configuration of the board as Host or Client in function of the connection wire used for linking both devices (SMARC iMX8M and external device).

There is used the differential pair USB0 as USB 2.0 connection pins, and USB3 differential lines as USB 3.0 connection pins (differential pairs USB3_SSTX and USB3_SSRX, SuperSpeed USB data).

Control lines are USB0_OTG_ID (to detect what kind of device is connected; active high) and USB0_VBUS_DET (host power detection, when this port is used as a device).

The last used pin is USB0_EN_OC#, who acts as enable bidirectional pin. Be careful when implement over-current function to avoid any short-circuit in this pin.

- **USB 3.0 Host:**

The second USB connection uses differential pair USB1 as USB 2.0, and USB2 as USB 3.0 in the same way as the first one. As commented, the reason to use this configuration is because in case of two USB ports it is mandatory use the USB1.

For the same reason, according the SMARC standard, this port must be Host and there are not used the pins type VBUS_DET and OTG_ID (it is not possibility to have a speed OTG detection by hardware; anyway, it is also possible to have the OTG functions, Host and Client, configured by software).

Be careful, when implement over-current function, to avoid any short circuit in pin USB1_EN_OC#.

Following table offers the list of related pins in the SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
USB 3.0 OTG				
P60	USB	I/O CMOS	USB0+	UBS1: USB2.0 differential data input.
P61	USB	I/O CMOS	USB0-	UBS1: USB2.0 differential data input.
P62	3V3	I/O OD CMOS	USB0_EN_OC#	USB1: USB2.0 enable pin. Active low. Related to GPIO1_13 (iMX8M processor ball K6).
P63	5V	I CMOS	USB0_VBUS_DET	USB1: USB2.0 Host power detection when this port is used as a device.
P64	3V3	I CMOS	USB0_OTG_ID	USB1: Input Pin to Announce OTG ID (Device Insertion) on USB 2.0 Port.
S62	USB SS	O CMOS	USB3_SSTX+	USB1 SS: TX differential pair.
S63	USB SS	O CMOS	USB3_SSTX-	USB1 SS: TX differential pair.
S65	USB SS	I CMOS	USB3_SSRX+	USB1 SS: RX differential pair.
S66	USB SS	I CMOS	USB3_SSRX-	USB1 SS: RX differential pair.
USB 3.0 Host				
P65	USB	I/O CMOS	USB1+	UBS2: USB2.0 differential data input.
P66	USB	I/O CMOS	USB1-	UBS2: USB2.0 differential data input.
P67	3V3	I/O OD CMOS	USB1_EN_OC#	USB2: USB2.0 enable pin. Active low. Related to GPIO1_15 (iMX8M processor ball J6).
S37	5V	I CMOS	USB3_VBUS_DET	USB3: USB2.0 Host power detection when this port is used as a device.
S71	USB SS	O CMOS	USB2_SSTX+	USB2 SS: TX differential pair.
S72	USB SS	O CMOS	USB2_SSTX-	USB2 SS: TX differential pair.
S74	USB SS	I CMOS	USB2_SSRX+	USB2 SS: RX differential pair.
S75	USB SS	I CMOS	USB2_SSRX-	USB2 SS: RX differential pair.

Table 12 USB pins

For **USB implementation examples**, you could consult the SMARC Design Guide 2.0 (page 64).

5.5 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

The SMARC iMX8M module can be connected to other peripheral devices using functionality of a standard I2C master and slave. I2C is a two wire, bidirectional serial bus which offers an easy interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.
There are four I2C ports and, according the SMARC standard, all of them has a primary purpose and an alternate use.

- **I2C_PM (I2C 2)**

To be used, as primary purpose, in Power Management functions. A usual function is to control a serial EEPROM in the Carrier Board allowing to read Carrier Board parameters.

- **I2C_GP (I2C 1)**

General purpose I2C bus.

- **I2C_CAM0 (I2C 3)**

Camera support: either connecting an I2C camera (using MIPI-CSI 2.0) or as differential data lane to communicate with camera (CSI0_TX+/-, using MIPI-CSI 3.0). This also can be used as general purpose I2C bus.

- **I2C_CAM1 (I2C 4)**

Camera support: either connecting an I2C camera (using MIPI-CSI 2.0) or as differential data lane to communicate with camera (CSI1_TX+/-, using MIPI-CSI 3.0). This also can be used as general purpose I2C bus. In the SMARC connector, it can be found in S1 and S2 pins, as well as S139 and S140 pins.

The next table is shown all the I2c pins:

Pin	Volt Level	Type	Main Function	Comments
P121	1V8	I/O OD CMOS	I2C_PM_CK	Power management I2C bus CLK
P122	1V8	I/O OD CMOS	I2C_PM_DAT	Power management I2C bus DATA
S1	1V8	IO OD CMOS	I2C_CAM1_CK	I2C4: Clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S2	1V8	IO OD CMOS	I2C_CAM1_DATA	I2C 4: Data signal. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S5	1V8	IO OD CMOS	I2C_CAM0_CK	I2C 3: Clock. Serial camera support link for serial cameras. Alternate function: CSI_TX+
S7	1V8	IO OD CMOS	I2C_CAM0_DAT	I2C 3: Data signal. Serial camera support link for serial cameras. Alternate function: CSI_TX-
S48	1V8	I/O OD CMOS	I2C_GP_CK	I2C1: Clock signal.
S49	1V8	I/O OD CMOS	I2C_GP_DAT	I2C1: Data signal.
S139	1V8	I/O CMOS	I2C_LCD_CK	I2C4 Clock to Read LCD Display EDID EEPROMs
S140	1V8	I/O CMOS	I2C_LCD_DAT	I2C4 Data to Read LCD Display EDID EEPROMs

Table 13 I2C pins

For **I2C implementation examples**, you could consult the SMARC Design Guide 2.0 (page 45).

5.6 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the module to external peripherals. The SMARC iMX8M module uses the Enhanced Configurable Serial Peripheral Interface (ECSPI). This is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

SMARC iMX8M uses a 1,8 V voltage levels for ECSPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs. There are available up to two ECSPI buses. The first one (ECSPI1) is only present in models without WiFi functionality. In this case, user have to be careful because this function is shared with UART3 (it is only possible to use one functionality: UART3 or ECSPI1).

The table below show all the SPI pins in the SMARC connector:

Pin	Volt Level	Type	Main Function	Comments
SPI0				
P31	1V8	O CMOS	SPI0_CS1#	SPI0 Master Chip Select 1. Related to GPIO3_20 (iMX8M processor ball L5).
P43	1V8	O CMOS	SPI0_CS0#	SPI0 Master Chip Select 0
P44	1V8	O CMOS	SPI0_CK	SPI0 Clock
P45	1V8	I CMOS	SPI0_DIN	SPI0 Master data input
P46	1V8	O CMOS	SPI0_DO	SPI0 Master data output
SPI1				
P54	1V8	O CMOS	SPI1_CS0#	SPI1 Master Chip Select 0
P56	1V8	O CMOS	SPI1_CK	SPI1 Clock
P57	1V8	I CMOS	SPI1_IO_0	SPI1 Master data input
P58	1V8	O CMOS	SPI1_IO_1	SPI1 Master data output

Table 14 SPI pins

For **SPI implementation examples**, you could consult the SMARC Design Guide 2.0 (page 59).

5.7 WiFi/Bluetooth and SD/MMC/SDIO CARD (4 bit) INTERFACE

The SMARC iMX8M modules contains a certified high-performance WiFi/Bluetooth module with Texas Instruments chipset. Main features are next:

- IEEE 802.11 b/g/n
- Bluetooth 4.2
- Module has an internal antenna.
- Possible to use an external antenna through U.FL jack connector.
- Using external antenna, the cable connected to module must have 50 Ω impedance.

This feature uses control lines from iMX8M processor which are shared with other peripheral.

- **UART3**

This is used to communicate with Bluetooth signals in the WiFi/Bluetooth module (BT_RX, BT_CTS, BT_TX and BT_RTS). If the module does not implement the WiFi/Bluetooth functionality, this can be used as SER2 or ECSPI1. These pins should be float if WiFi/Bluetooth is implemented.

- **SD2 interface**

This can be used, through a switch, to the SDIO input/outputs in the WiFi/Bluetooth module. If there is not implemented, it will be available in the SMARC-314 interface as SDIO interface. These pins should be float if WiFi/Bluetooth is implemented.

- **SAI3 interface**

This is also used to control the WiFi/Bluetooth module. If there is not present this function, it is available to use the bus I2S1 in the SMARC-314 interface. These pins should be float if WiFi/Bluetooth is implemented.

In models without WiFi/Bluetooth, it is possible to use the SD/MMC/SDIO interface to install a micro-SD card reader on the Carrier Board. This controller can only support up to 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 8 V and 3.3 V operation, but do not support 1.2 V operation.
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode.
- Up to SDR104 rate.

The use of a micro-SD, because this function shares some pins with WiFi/Bluetooth SDIO, is only present in all models without WiFi/Bluetooth connectivity and in models with WiFi/Bluetooth connectivity during Boot process.

The table below show all the SPI pins in the SMARC connector:

Pin	Volt Level	Type	Main Function	Comments
P33	3V3	I OD CMOS	SDIO_WP	SDIO card 4-bit Interface: Write Protect.
P34	3V3	I/O CMOS	SDIO_CMD	SDIO card 4-bit Interface: Command Line.
P35	3V3	I OD CMOS	SDIO_CD#	SDIO card 4-bit Interface: Card Detect.
P36	3V3	O CMOS	SDIO_CK	SDIO card 4-bit Interface: Clock.
P37	3V3	O CMOS	SDIO_PWR_EN	SDIO card 4-bit Interface: Card Power Enable.
P39	3V3	I/O CMOS	SDIO_D0	SDIO card 4-bit Interface: data path (D0).
P40	3V3	I/O CMOS	SDIO_D1	SDIO card 4-bit Interface: data path (D1).
P41	3V3	I/O CMOS	SDIO_D2	SDIO card 4-bit Interface: data path (D2).
P42	3V3	I/O CMOS	SDIO_D3	SDIO card 4-bit Interface: data path (D3).

Table 15 SDIO Card Interface pins

5.8 UART: ASYNCHRONOUS SERIAL PORTS

There are four asynchronous serial ports defined, some of which are shared with other peripherals. These can be with two or four wires. Available serial ports are next (named according SMARC specification and, in parentheses, the used port from iMX8M processor).

- **SER0 (UART1)**

Four wire port: two data lines and two handshake lines.

- **SER1 (UART2)**

Two wire port (data only).

- **SER2 (UART3)**

Four wire port. It is only present in all models without WiFi/Bluetooth connectivity (see also chapter 5.7 WiFi/BLUETOOTH AND SD/MMC/SDIO CARD INTERFACE). At the same time, when it is possible, it is a function shared with SPI1, so it is only possible to be used one of booth functions (see also chapter 5.6 SPI: SERIAL PERIPHERAL INTERFACE).

- **SER3 (UART4)**

Two wire port (data only).

The next table is shown all the UART pins:

Pin	Volt Level	Type	Main Function	Comments
P129	1V8	O CMOS	SER0_TX	UART1: Asynchronous serial port 1 data out.
P130	1V8	I CMOS	SER0_RX	UART1: Asynchronous serial port 1 data in.
P131	1V8	O CMOS	SER0_RTS#	UART1: Request to Send handshake line. Active low.
P132	1V8	I CMOS	SER0_CTS#	UART1: Clear to Send handshake line. Active low.
P134	1V8	O CMOS	SER1_TX	UART2: Asynchronous serial port 1 data out.
P135	1V8	I CMOS	SER1_RX	UART2: Asynchronous serial port 1 data in.
P136	1V8	O CMOS	SER2_TX	UART3: Asynchronous serial port 1 data out.
P137	1V8	I CMOS	SER2_RX	UART3: Asynchronous serial port 1 data in.
P138	1V8	O CMOS	SER2_RTS#	UART3: Request to Send handshake line. Active low.
P139	1V8	I CMOS	SER2_CTS#	UART3: Clear to Send handshake line. Active low.
P140	1V8	O CMOS	SER3_TX	UART4: Asynchronous serial port 1 data out.
P141	1V8	I CMOS	SER3_RX	UART4: Asynchronous serial port 1 data in.

Table 16 Asynchronous Serial Ports pins

For **UART implementation examples**, you could consult the SMARC Design Guide 2.0 (page 42).

5.9 I2S: SERIAL AUDIO PORT

The I2S (Inter IC Sound) is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally, PCM audio data is transmitted over the I2S interface. There are three I2S defined, which each one provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization.

In models with WiFi/Bluetooth connectivity there are only available two I2S ports: I2S1 is used for control purposes. This I2S1 port is only available in all models without WiFi/Bluetooth function (see also chapter 5.7 WiFi/BLUETOOTH AND SD/MMC/SDIO CARD INTERFACE).

Now a table that include all the I2S pins.

Pin	Volt Level	Type	Main Function	Comments
S38	1V8	O CMOS	AUDIO_MCK	SAI2: Master Clock output to Audio codecs.
S39	1V8	I/O CMOS	I2S0_LRCK	SAI2: Left & Right Audio synchronization clock.
S40	1V8	O CMOS	I2S0_SDOUT	SAI2: Digital Audio output.
S41	1V8	I CMOS	I2S0_SDIN	SAI2: Digital Audio input.
S42	1V8	I/O CMOS	I2S0_CK	SAI2: Digital Audio clock.
S43	1V8	I/O CMOS	I2S1_LRCK	SAI3: Left & Right Audio synchronization clock. (1)
S44	1V8	O CMOS	I2S1_SDOUT	SAI3: Digital Audio output. (1)
S45	1V8	I CMOS	I2S1_SDIN	SAI3: Digital Audio input. (1)
S46	1V8	I/O CMOS	I2S1_CK	SAI3: Digital Audio clock. (1)
S50	1V8	I/O CMOS	I2S2_LRCK	SAI1: Left & Right Audio synchronization clock.
S51	1V8	O CMOS	I2S2_SDOUT	SAI1: Digital Audio output.
S52	1V8	I CMOS	I2S2_SDIN	SAI1: Digital Audio input.
S53	1V8	I/O CMOS	I2S2_CK	SAI1: Digital Audio clock.
S93	1V8	O CMOS	DP0_LANE 0+/SAI1_MCLK	SAI1: Primary DP Port Differential
S94	1V8	O CMOS	DP0_ LANE 0-/SAI1_TXD1	SAI1: Primary DP Port Differential
S95	1V8	I CMOS	DP0_SEL/SAI1_TXD2	SAI1: DP Selection
S96	1V8	O CMOS	DP0_ LANE 1+/SAI1_TXD3	SAI1: Primary DP Port Differential.
S97	1V8	O CMOS	DP0_ LANE 1-/SAI1_TXD4	SAI1: Primary DP Port Differential.
S98	1V8	I CMOS	DP0_HDP/SAI1_TXD5	SAI1: DP Hot Plug detect input.
S99	1V8	O CMOS	DP0_LANE 2+/SAI1_TXD6	SAI1: Primary DP Port Differential.

S100	1V8	O CMOS	DP0_LANE 2-/SAI1_TXD7	SAI1: Primary DP Port Differential.
S102	1V8	O CMOS	DP0_LANE 3+/SAI1_RXD1	SAI1: Primary DP Port Differential.
S103	1V8	O CMOS	DP0_LANE 3-/SAI1_RXD2	SAI1: Primary DP Port Differential.
S104	3V3	I CMOS	USB3_OTG_ID/SAI1_RXD3	SAI1: Primary DP Port Differential /USB2.0 OTG ID input.
S105	3V3	I/ O CMOS	DP0_X+/SAI1_RXD4	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control
S106	3V3	I/ O CMOS	DP0_X-/SAI1_RXD5	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control
S107	1V8	O CMOS	LCD1_BKLT_EN	SAI1: Secondary Panel Backlight Enable
S108	DS	O CMOS	LVDS1-eDSI1-DSII_CK+	SAI1: Secondary LVDS Channel Differential Pair Clock Lines
S109	DS	O CMOS	LVDS1-eDSI1-DSII_CK-	SAI1: Secondary LVDS Channel Differential Pair Clock Lines
S111	DS	O CMOS	LVDS1-eDSI1-DSII_0-	SAI1: Secondary LVDS Channel Differential Pair Data Lines
S141	1V8	O CMOS	LCD0_BKLT_PWM	SAI3: LCD Primary Panel Brightness Control. Related to GPIO5_2(iMX8M processor ball D3)

Table 17 I2S Interface pins

For **I2S implementation examples**, you could consult the SMARC Design Guide 2.0 (page 56).

5.10 HDMI DISPLAY

High-Definition Multimedia Interface is an audio/video interface for transmitting uncompressed video data and compressed or uncompressed digital audio data from an HDMI-compliant source device, such as a display controller, to a compatible computer monitor, video projector, digital television, or digital audio device. HDMI is a digital replacement for analog video standards. This output serial bus is composed by:

- Three data differential pairs.
- One differential clock output pair.
- Two I2C dedicated lines (data and clock) as control signals.
- A Hot Plug detect input and a CEC line.

Pin	Volt Level	Type	Main Function	Comments
P92	TMDS HDMI	O CMOS	HDMI_D2+	HDMI differential data input D2.
P93	TMDS HDMI	O CMOS	HDMI_D2-	HDMI differential data input D2.
P95	TMDS HDMI	O CMOS	HDMI_D1+	HDMI differential data input D1.
P96	TMDS HDMI	O CMOS	HDMI_D1-	HDMI differential data input D1.
P98	TMDS HDMI	O CMOS	HDMI_D0+	HDMI differential data input D0.
P99	TMDS HDMI	O CMOS	HDMI_D0-	HDMI differential data input D0.
P101	TMDS HDMI	O CMOS	HDMI_CK+	HDMI differential clock output pair. Clock Lines
P102	TMDS HDMI	O CMOS	HDMI_CK-	HDMI differential clock output pair. Clock Lines
P104	1V8	I CMOS	HDMI_HPD	HDMI Hot Plug detect input.
P105	1V8	I/O OD CMOS	HDMI_CTRL_CK	I2C Clock line dedicated to HDMI.
P106	1V8	I/O OD CMOS	HDMI_CTRL_DAT	I2C Data line dedicated to HDMI.
P107	1V8	I/O CMOS	HDMI_CEC	CEC Consumer Electronic Control.

Table 18 HDMI pins

For **HDMI implementation examples**, you could consult the SMARC Design Guide 2.0 (page 38).

5.11 MIPI-DSI: DISPLAY SERIAL INTERFACE

The SMARC iMX8M has available a 4-lanes DSI port. The Display Serial Interface (DSI) is a specification by the Mobile Industry Processor Interface (MIPI) Alliance, aimed at reducing the cost of display controllers in a mobile device. It is commonly targeted at LCD and similar display technologies. It defines a serial bus and a communication protocol between the host (source of the image data) and the device (destination of the image data).

Also, there are available three LCD control pins: Power Enable, Backlight Enable and Backlight PWM. These and DSI pins are explained in the table below:

Pin	Volt Level	Type	Main Function	Comments
S125	DS	O CMOS	DSI0_D0+	DSI: Data pair 0.
S126	DS	O CMOS	DSI0_D0-	DSI: Data pair 0.
S128	DS	O CMOS	DSI0_D1+	DSI: Data pair 1.
S129	DS	O CMOS	DSI0_D1-	DSI: Data pair 1.
S131	DS	O CMOS	DSI0_D2+	DSI: Data pair 2.
S132	DS	O CMOS	DSI0_D2-	DSI: Data pair 2.
S134	1V8	I/O CMOS	DSI0_CLK+	DSI: Clock pair.
S135	1V8	I/O CMOS	DSI0_CLK-	DSI: Clock pair.
S137	DS	O CMOS	DSI0_D3+	DSI: Data pair 3.
S138	DS	O CMOS	DSI0_D3-	DSI: Data pair 3.
LCD Controls				
S127	1V8	O CMOS	LCD0_BKLT_EN	SAI3: LCD Primary Panel Backlight Enable.
S133	1V8	O CMOS	LCD0_VDD_EN	LCD Primary Panel Power Enable. Related to GPIO3_9 (iMX8M processor ball J21)
S141	1V8	Output	LCD0_BKLT_PWM	LCD Backlight PWM. Related to GPIO5_2/PWM4 (imx8M processor ball D3)

Table 19 MIPI-DSI pins

For **MIPI-DSI implementation examples**, you could consult the SMARC Design Guide 2.0 (page 41).

5.12 DP: Display Port

DisplayPort is a digital display interface used to connect a video source to a display device such as a computer monitor, and it can also carry audio, USB, and other forms of data. The interface is backward compatible with other interfaces, such as HDMI and DVI, through the use of either active or passive adapters. So, HDMI pins may alternatively be used for DP operation.

DisplayPort can directly output HDMI and DVI signals. The level adaptation can be implemented on the Carrier or via plug in cable adapter. In case of Carrier Board implementation, a level shifter adjusts the I/O voltage to HDMI/DVI compliant signal levels. A dual-mode chipset switches to DVI/HDMI mode (4-lane main DisplayPort link and AUX channel) if a DVI or HDMI passive adapter is detected (by DP0_AUX_SEL), as we can see on the next pins table:

Pin	Volt Level	Type	Main Function	Comments
P92	TMDS HDMI	O CMOS	HDMI_D2+/DP1_LANE0+	HDMI differential data input D2.
P93	TMDS HDMI	O CMOS	HDMI_D2-/DP1_LANE0-	HDMI differential data input D2.
P95	TMDS HDMI	O CMOS	HDMI_D1+/DP1_LANE1+	HDMI differential data input D1.
P96	TMDS HDMI	O CMOS	HDMI_D1-/DP1_LANE1-	HDMI differential data input D1.
P98	TMDS HDMI	O CMOS	HDMI_D0+/DP1_LANE2+	HDMI differential data input D0.
P99	TMDS HDMI	O CMOS	HDMI_D0-/DP1_LANE2-	HDMI differential data input D0.
P101	TMDS HDMI	O CMOS	HDMI_CK+/DP1_LANE3+	HDMI differential clock output pair.
P102	TMDS HDMI	O CMOS	HDMI_CK-/DP1_LANE3-	HDMI differential clock output pair.
P104	1V8	I CMOS	HDMI_HPD/DP1_HPD	HDMI Hot Plug detect input.
P105	1V8	I/O OD CMOS	HDMI_CTRL_CK/DP1_X+	I2C Clock line dedicated to HDMI.
P106	1V8	I/O OD CMOS	HDMI_CTRL_DAT/DP1_X-	I2C Data line dedicated to HDMI.
P107	1V8	I/O CMOS	HDMI_CEC/DP1_SEL	CEC Consumer Electronic Control.
S93	1V8	O CMOS	DP0_ LANE 0+/SAI1_MCLK	SAI1: Primary DP Port Differential
S94	1V8	O CMOS	DP0_ LANE 0-/SAI1_TXD1	SAI1: Primary DP Port Differential
S95	1V8	I CMOS	DP0_SEL/SAI1_TXD2	SAI1: DP Selection
S96	1V8	O CMOS	DP0_ LANE 1+/SAI1_TXD3	SAI1: Primary DP Port Differential.
S97	1V8	O CMOS	DP0_ LANE 1-/SAI1_TXD4	SAI1: Primary DP Port Differential.
S98	1V8	I CMOS	DP0_HDP/SAI1_TXD5	SAI1: DP Hot Plug detect input.

S99	1V8	O CMOS	DP0_ LANE 2+/SAI1_TXD6	SAI1: Primary DP Port Differential.
S100	1V8	O CMOS	DP0_ LANE 2-/SAI1_TXD7	SAI1: Primary DP Port Differential.
S102	1V8	O CMOS	DP0_ LANE 3+/SAI1_RXD1	SAI1: Primary DP Port Differential.
S103	1V8	O CMOS	DP0_ LANE 3-/SAI1_RXD2	SAI1: Primary DP Port Differential.
S105	3V3	I/ O CMOS	DP0_X+/SAI1_RXD4	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control
S106	3V3	I/ O CMOS	DP0_X-/SAI1_RXD5	SAI1: Primary DP Port Bidirectional Channel used for Link Management and Device Control

Table 20 DP pins

For **DP implementation examples**, you could consult the SMARC Design Guide 2.0 (page 39).

5.13 MIPI-CSI: CAMERA SERIAL INTERFACE

There are defined two MIPI-CSI camera serial interfaces. Both support MIPI-CSI 2.0 but they are also prepared to support MIPI-CSI 3.0. Main difference is that MIPI-CSI 2.0 uses an I2C bus to communicate with camera (pins I2C_CAM[0:1]) and MIPI-CSI 3.0 uses a differential data lane (alternative function of the same pins, CSI[0:1]_TX+/-).

These two buses are implemented with 4 lanes. For each bus, there are also available two lines of Power Enable and Reset, in shared pins with GPIOs. We can see all these pins in the table below:

Pin	Volt Level	Type	Main Function	Comments
P3	LVDS D-PHY	Input	CSI1_CK+	CSI1 differential Clock input.
P4	LVDS D-PHY	Input	CSI1_CK-	CSI1 differential Clock input.
P7	LVDS D-PHY	Input	CSI1_RX0+	CSI1 D0 differential data input.
P8	LVDS D-PHY	Input	CSI1_RX0-	CSI1 D0 differential data input.
P10	LVDS D-PHY	Input	CSI1_RX1+	CSI1 D1 differential data input.
P11	LVDS D-PHY	Input	CSI1_RX1-	CSI1 D1 differential data input.
P13	LVDS D-PHY	Input	CSI1_RX2+	CSI1 D2 differential data input.
P14	LVDS D-PHY	Input	CSI1_RX2-	CSI1 D2 differential data input.
P16	LVDS D-PHY	Input	CSI1_RX3+	CSI1 D3 differential data input.
P17	LVDS D-PHY	Input	CSI1_RX3-	CSI1 D3 differential data input.
S6	1V8	Output	CAM_MCK	Master clock for CSI camera support (may be used for CSI1 and CSI2).
S8	LVDS D-PHY	Input	CSI0_CK+	CSI2 differential Clock input.
S9	LVDS D-PHY	Input	CSI0_CK-	CSI2 differential Clock input.

S11	LVDS D-PHY	Input	CSI0_RX0+	CSI2 D0 differential data input.
S14	LVDS D-PHY	Input	CSI0_RX0-	CSI2 D0 differential data input.
S14	LVDS D-PHY	Input	CSI0_RX1+	CSI2 D1 differential data input.
S15	LVDS D-PHY	Input	CSI0_RX1-	CSI2 D1 differential data input.
S29	LVDS D-PHY	I CMOS	CSI2_D2+	CSI1 D2 differential data input.
S30	LVDS D-PHY	I CMOS	CSI2_D2-	CSI1 D2 differential data input.
S32	LVDS D-PHY	I CMOS	CSI2_D3+	CSI1 D3 differential data input.
S33	LVDS D-PHY	ICMOS	CSI2_D3-	CSI1 D3 differential data input.

Table 21 MIPI-CSI pins

For **MIPI-CSI implementation examples**, you could consult the SMARC Design Guide 2.0 (page 87).

5.14 PCIe: PCI EXPRESS

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high-speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out only x1 operation. A PCIe link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for only PCIe transmit pair.

In the SMARC iMX8M there are two PCIe links (PCIeA and PCIeB). These are configured as one single lane link. Each PCI Express port requires an external 100MHz PCIe compliant reference clock.

The next table shows all PCIe SMARC pins:

Pin	Volt Level	Type	Main Function	Comments
P73	3V3	I CMOS	PCIE_B_PRSNT#	PCIeB: Hotplug presence detect. Active low. Related to GPIO1_3 (iMX8M processor ball P4).
P74	3V3	I CMOS	PCIE_A_PRSNT#	PCIeA: Hotplug presence detect. Active low. Related to GPIO1_3 (iMX8M processor ball P4).
P75	3V3	I CMOS	PCIE_A_RST#	PCIeA: Port reset output. Active low. Related to GPIO1_10 (iMX8M processor ball M7).
P77	3V3	IO OD CMOS	PCIE_B_CKREQ#	PCIe Port B clock request. Associated with GPIO5_21 (iMX8M processor ball F9).
P78	3V3	O OD CMOS	PCIE_A_CKREQ#	PCIe Port A clock request. Associated with GPIO5_20 (iMX8M processor ball F8).
P83	LVDS PCIe	O CMOS	PCIE_A_REFCK+	PCIeA: Differential PCIe Link reference clock output DC coupled.
P84	LVDS PCIe	O CMOS	PCIE_A_REFCK-	PCIeA: Differential PCIe Link reference clock output DC coupled.
P86	LVDS PCIe	I CMOS	PCIE_A_RX+	PCIeA: Differential PCIe Link receive data pair 0
P87	LVDS PCIe	I CMOS	PCIE_A_RX-	PCIeA: Differential PCIe Link receive data pair 0

P89	LVDS PCIe	O CMOS	PCIE_A_TX+	PCIeA: Differential PCIe Link transmit data pair 0
P90	LVDS PCIe	O CMOS	PCIE_A_TX-	PCIeA: Differential PCIe Link transmit data pair 0
S76	3V3	O CMOS	PCIE_B_RST#	PCIeB: Port reset output. Active low. Related to GPIO1_3
S84	LVDS PCIe	O CMOS	PCIE_B_REFCK+	PCIeB: Differential PCIe Link reference clock output DC coupled.
S85	LVDS PCIe	O CMOS	PCIE_B_REFCK-	PCIeB: Differential PCIe Link reference clock output DC coupled.
S87	LVDS PCIe	I CMOS	PCIE_B_RX+	PCIeB: Differential PCIe Link receive data pair 0
S88	LVDS PCIe	I CMOS	PCIE_B_RX-	PCIeB: Differential PCIe Link receive data pair 0
S90	LVDS PCIe	O CMOS	PCIE_B_TX+	PCIeB: Differential PCIe Link transmit data pair 0
S91	LVDS PCIe	O CMOS	PCIE_B_TX-	PCIeB: Differential PCIe Link transmit data pair 0
S146	3V3	I OD CMOS	PCIE_WAKE	PCIe wake up interrupt to host. Common to PCIe links A, B. Related to GPIO1_7 (iMX8M processor ball N6).

Table 22 PCI Express pins

5.15 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. These can be configured as either inputs or outputs.

- When configured as an output: It is possible to write an internal register to control the state driven on the output pin.
- When configured as an input: It is possible to detect the state of the input by reading the state of an internal register.

Pin	Volt Level	Type	Main Function	Comments
P108	1V8	I/O CMOS	GPIO0/CAM0_PWR#	SMARC GPIO pin. Related to NAND_GPIO3_0 (iMX8M-NAND processor ball G19).
P109	1V8	I/O CMOS	GPIO1/CAM1_PWR#	SMARC GPIO pin. Related to NAND_GPIO3_1 (iMX8M-NAND processor ball H19).
P110	1V8	I/O CMOS	GPIO2/CAM0_RST#	SMARC GPIO pin. Related to NAND_GPIO3_2 (iMX8M-NAND processor ball G21).
P111	1V8	I/O CMOS	GPIO3/CAM1_RST#	SMARC GPIO pin. Related to NAND_GPIO3_3 (iMX8M-NAND processor ball F21).
P112	1V8	I/O CMOS	GPIO4/HDA_RST#	SMARC GPIO pin. Related to NAND_GPIO3_4 (iMX8M-NAND processor ball H20).

P113	1V8	I/O CMOS	GPIO5/PWM_OUT	SMARC GPIO pin. Related to SPDIFIX_GPIO5_3_PWM3(iMX8M-SAI processor ball F6).
P114	1V8	I/O CMOS	GPIO6/TACHIN	SMARC GPIO pin. Related to NAND_GPIO3_5(iMX8M-NAND processor ball H21).
P115	1V8	I/O CMOS	GPIO7/PCAM_FLD	SMARC GPIO pin. Related to NAND_GPIO3_14 (iMX8M-NAND processor ball M20).
P116	1V8	I/O CMOS	GPIO8/CAN0_ERR#	SMARC GPIO pin. Related to NAND_GPIO3_15 (iMX8M processor ball K19).
P117	1V8	I/O CMOS	GPIO9/CAN_ERR#	SMARC GPIO pin. Related to NAND_GPIO3_16 (iMX8M-NAND processor ball K20).
P118	1V8	I/O CMOS	GPIO10	SMARC GPIO pin. Related to NAND_GPIO3_17 (iMX8M-NAND processor ball K22).
P119	1V8	I/O CMOS	GPIO11	SMARC GPIO pin. Related to NAN_GPIO3_18(iMX8M-NAND processor ball K21).
S133	1V8	O CMOS	LCD0_VDD_EN	SMARC GPIO pin. Related to GPIO3_9_LCD_EN (iMX8M processor ball J21)

Table 23 GPIO pins

5.16 RTC BATTERY

In the SMARC connector is an input available to use and RTC backup power. The User will implement a Lithium Cell or Super-Cap in a voltage range between 2,0 V and 3,25 V (it is recommended to use a standard Lithium Cell of 3,0 V). This pin can be left open if RTC functions are not required.

The Carrier Board must be implemented the needed circuits to protect against charging by reverse currents.

Pin	Volt Level	Type	Main Function	Comments
S147	3V	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.

Table 24 RTC pin

For **RTC Battery implementation examples**, you could consult the SMARC Design Guide 2.0 (page 31).

5.17 ENVIRONMENTAL SPECIFICATION

General Specification	Operating	Non-operating
Industrial grade (E2)	-40ºC to +80ºC	-40ºC to +80ºC

Table 25 Temperature range

Standard modules are available for Industrial grade temperature range. The operating temperature is the maximum measurable temperature on any spot on the module's surface.

- **Humidity**

93% relative Humidity at 40ºC, non-condensing (according to IEC 60068-2-78).

5.18 STANDARDS AND CERTIFICATIONS

- **RoHS**

The SMARC iMX8M is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

- **CE Marking**

The SMARC iMX8M is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

- **WEEE Directive**

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

- **Conformal Coating**

Conformal Coating is available for Computer-on-Modules and for validated SMARC modules. Please, contact your local sales or support for further details.

- **EMC**

The SMARC iMX8M is designed and tested following EN55022 standard ("INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT").

- **SMARC Form Factor standard**

The SMARC (“Smart Mobility Architecture”) is a versatile small form factor computer Module definition targeting application that require low power, low costs and high performance.

5.19 MTBF

The SMARC iMX8M has been designed with a predicted MTBF (Mean Time Before Failure) of >131400 hours (>15 years).

All hardware components are selected with long time industrial reliability parameters. The MTBF prediction of hardware components and temperature stress could be estimated, but the newest devices are very software dependent. So, final application has an important effect on MTBF.

5.20 MECHANICAL SPECIFICATION

- **Module Dimension**

82,00 mm x 50,00 mm x 4,30 mm (high without JTAG connector)

- **Mechanical Drawing**

The next figures show the SMARC iMX8M modules mechanical dimensions:

  - All dimensions are in millimeters.
  - 10-layer Printed Circuit Board size is 82,00 mm x 50,00 mm x 1,15 mm.
  - Mounting holes are provided, one on each corner.

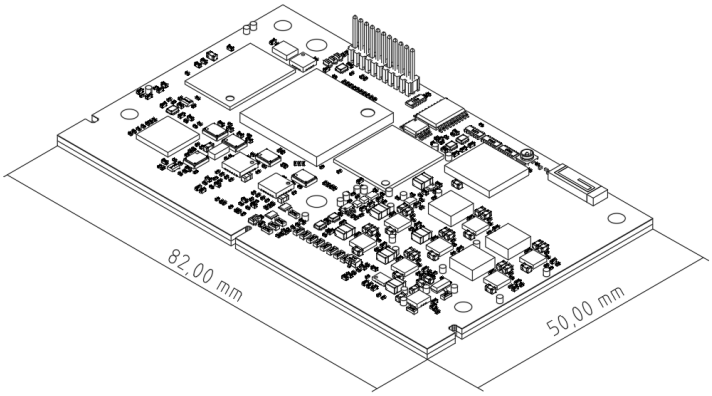

Figure 11 SMARC iMX8M Outline dimensions

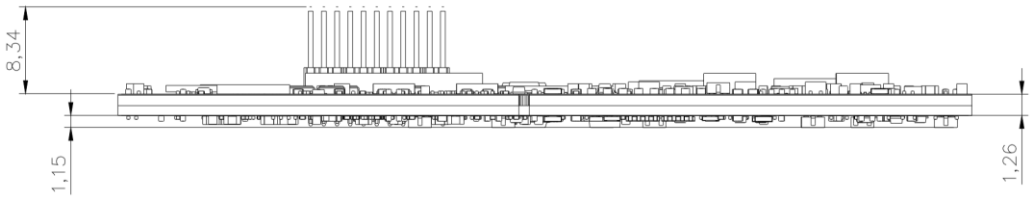

Figure 12 SMARC iMX8M Lateral view widths dimensions

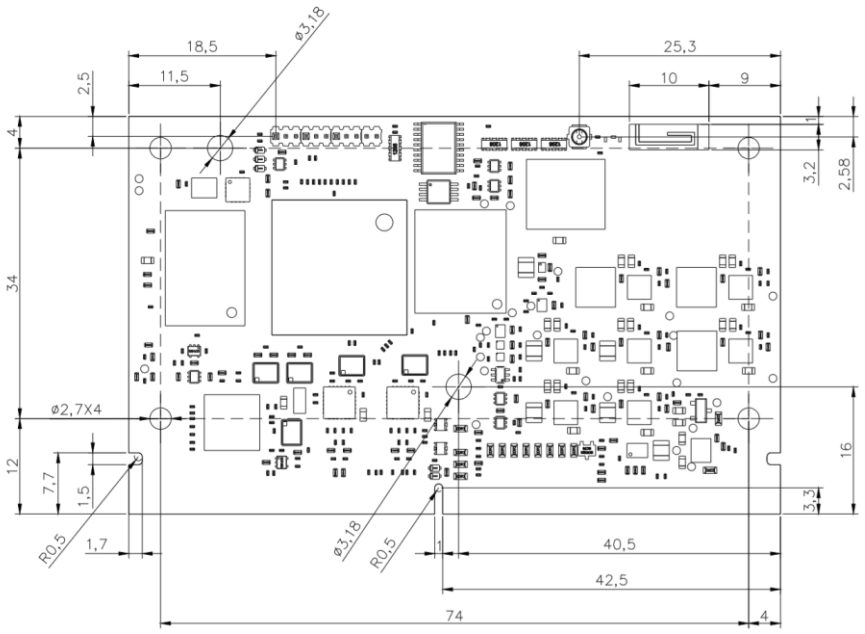

Figure 13 SMARC iMX8M Side view detailed mechanical dimension

6 ON-BOARD INTERFACES

6.1 SUMMARY

Device	Connector	Reference	Description
LEDs	-	DLED1 DLED2	GPIO controlled
JTAG	11-pin 1,25 mm pitch interface	JTAG	-

Table 26 Interface summary

6.2 LEDs

The SMARC iMX8M module provides two bicolor LED indicator on the board. They can be controlled by the user through GPIOs.

Signal Name	LED Color	Description
GPIO1_5	USER0 Red	Controlled by GPIO1_5 of iMX8M
SAI5_GPIO3_24	USER1 Green	Controlled by GPIO3_24 of iMX8M
GPIO1_8	USER2 Red	Controlled by GPIO1_8 of iMX8M
NAND_GPIO3_13_LED	USER3 Green	Controlled by GPIO3_13 of iMX8M

Table 27 LEDs

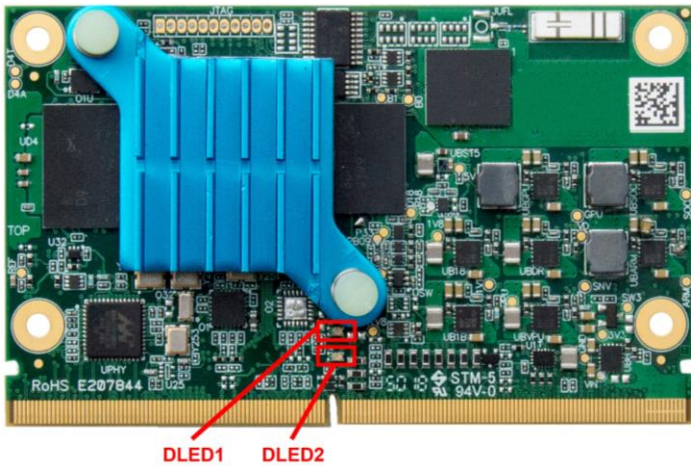

Figure 14 LEDs position in the PCB

6.3 JTAG

The SMARC iMX8M provides a footprint JTAG interface to help in the developing of user's code.

The JTAG port is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M4 and Cortex A53 Cores DAP - debug access port.

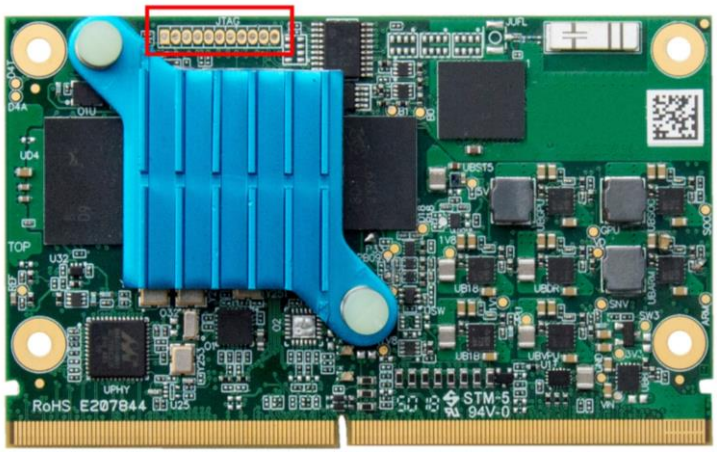

Figure 15 JTAG position in the PCB

Next figure shows the pinout schematic and the corresponding metal contacts.

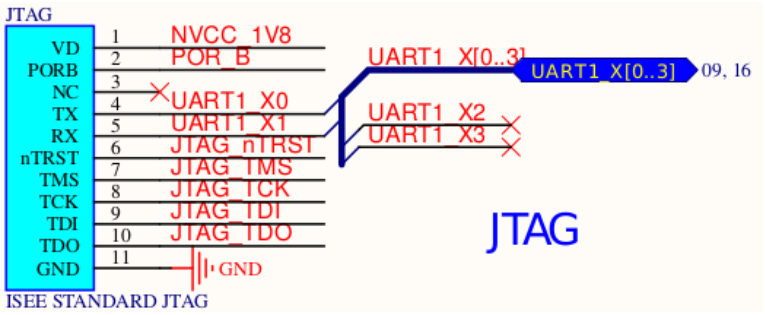

Figure 16 JTAG connector schematic

Note that even pins are left unconnected, but the footprint makes possible to use a 11 pin 1.27 mm pitch connector. Next table details the signals on each pin.

Signal Name	JTAG pin	Description
NVCC_1V8	1	1,8 V power supply.
POR_B	2	Processor iMX8M Cold Reset. Active Low.
NC	3	Not Connected.
UART1_X0	4	UART1: Asynchronous serial port 1 data out.
UART1_X1	5	UART1: Asynchronous serial port 1 data in.
JTAG_NTRST	6	JTAG Test Reset Input Signal.
JTAG_TMS	7	JTAG Test Mode Select Input Signal.
JTAG_TCK	8	JTAG Test Clock Input Signal.
JTAG_TDI	9	JTAG Test Data Input Signal.
JTAG_TDO	10	JTAG Test Data Output Signal.
GND	11	Ground.

Table 28 JTAG pinout

7 ELECTRICAL CHARACTERISTICS

Electrical parameter	Min	Typ	Max	Unit
5 V INPUT POWER SUPPLY				
SMARC iMX8M Input Power Supply Voltage	3.0	-	5.25	V
SMARC iMX8M Input Power Supply Current (1)	-	0.43	2	A
Input/Output pins (2)				
Output High-Level DC Voltage	1.6	-	1.8	V
Input High-Level DC Voltage	1.26	-	1.8	V
Output Low-Level DC Voltage	-	-	0.2	V
Input Low-Level DC Voltage	0	-	0.54	V
RTC_BATTERY type pins				
Input DC Voltage	2.5	3	3.25	V

Table 29 SMARC iMX8M Electrical Characteristics

(1) Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.

(2) The electrical specification depends on the configured mode. For accurate information of each pin, revise iMX8M Applications Processor official document from NXP official site https://www.nxp.com/

SMARC iMX8M MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED.

WARRANTY LOST IF IMPROPER USE OF THE MODULE IS FOUND.

8 EXPANSION BOARD

All the products in the SMARC iIMX8M series can be supplemented with next expansion board.

Part Number	IGEP™ Device	Description
BASE0040-DFEV-UGAC	BASE SMARC EXPANSION	Designed for fast prototyping of user's projects

Table 30 BASE SMARC EXPANSION Ordering Information

The BASE SMARC EXPANSION is a fully equipped baseboard that access to almost all SMARC functionalities. It has been designed to be used as the fastest way to develop and check the user's final application before building a prototype, saving costs and reducing time to market.

This model can be used with all the ISEE ASSEMBLY TECHNOLOGY's SMARC series modules. Thanks to this design, the user only needs to purchase one Expansion board to check all SMARC modules manufactured by ISEE ASSEMBLY TECHNOLOGY.

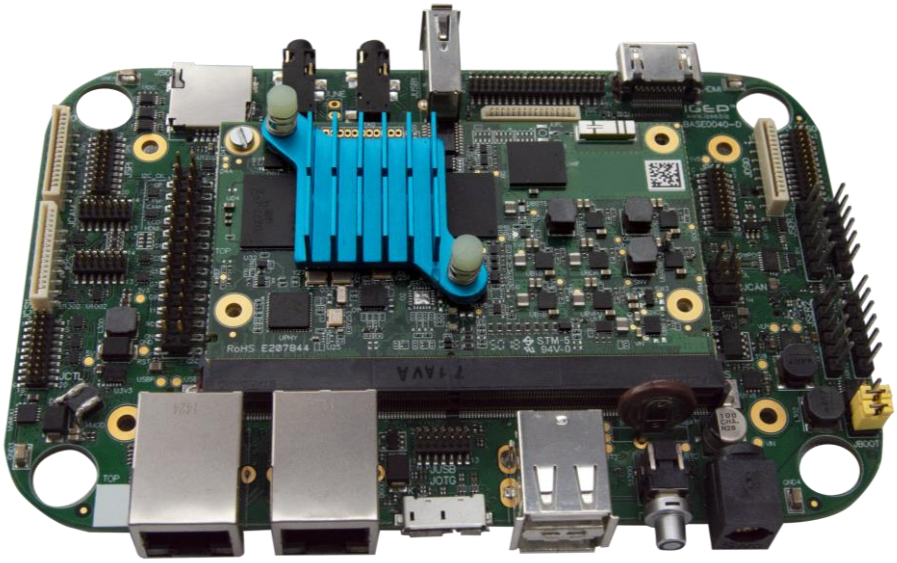

Figure 17 BASE0040 SMARC EXPANSION

The following table contains all the features and capabilities of the BASE SMARC EXPANSION.

Connectors	Features	Dimensions	Case Dimensions
1 x SMARC connector 1 x Power Supply (+5 V) connector 2 x 10/100/1000 Mbps Base RJ45 1 x HDMI Type A receptacle 1 x LCD 24-bit connector 1 x Touchscreen connector 1 x XLCD expansion 40-pin header 1 x LVDS expansion 24-pin header 2 x CSI connector, 2-lanes 1 x Parallel Camera expansion 14-pin header 1 x Stereo Line Input Mic/Line 1 x Stereo Line Output Headphone 1 x I2S 14-pin header 3 x USB 2.0 Type A receptacle 1 x USB 3.0 Type AB receptacle 1 x USB2 expansion 14-pìn header 1 x Modem USB & PCIe interface 1 x mSATA & PCIe interface 1 x PCI expansion 20-pin header 1 x Micro-SD connector 1 x SIM-card connector 2 x DSI connector 2 x CAN on a 6-pin header 1 x SPI 20-pin header 1 x I/O expansion 28-pin header 4 x Serial UART 3V3 expansion 6-pin header	1 x Button-LED (2 LEDs: red, blue) 3 x Boot jumpers 1 x Control 20-pin header	142,00 mm x 90,00 mm (without case)	150,00 mm x 100,00 mm x 30,00 mm

Table 31 BASE0040 SMARC EXPANSION Features Rev. D

9 Document and Standards References

- **CAN** (“Controller Area Network”) Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- **MIPI CSI-2** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **MIPI CSI-3** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **COM Express** – the formal title for the COM Express specification is “PICMG® COM.0 COM Express Module Base Specification”, Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG (“PCI Industrial Computer Manufacturer’s Group”) (www.picmg.org)
- **DisplayPort and Embedded DisplayPort -** These standards are owned and maintained by VESA (“Video Electronics Standards Association”) (www.vesa.org)
- **MIPI DSI** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **eMMC** (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- **eSPI** (“Enhanced Serial Peripheral Interface”) The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- **Fieldbus** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: https://www.profibus.com/download/ and www.can-cia.org
- **GBE MDI** (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **HDA (HD Audio),** High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (http://www.intel.com)
- **HDMI Specification,** Version 2.1, November 28, 2017 (www.hdmi.org)
- **I2C Specification,** Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (www.nxp.com)
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- **IEEE1588 - 2008**. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (http://standards.ieee.org)
- **JTAG** (“Joint Test Action Group”) This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (https://ieeexplore.ieee.org)
- **MXM3** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- **PICMG® EEEP** Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org)
- **PCI Express** Specifications (www.pci-sig.org)
- **Serial ATA** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org) SMARC 2.1.1 Specification © 2020 SGET e.V. Page 9 of 109
- **SD Specifications** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)
- **SM Bus** – “System Management Bus” Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (http://www.smbus.org)

- **SPI Bus** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- **USB** Specifications (http://www.usb.org)